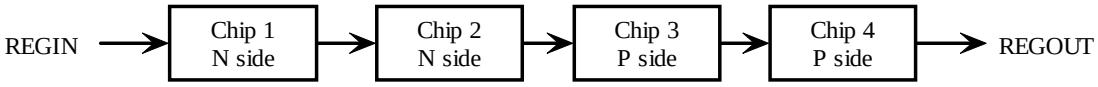
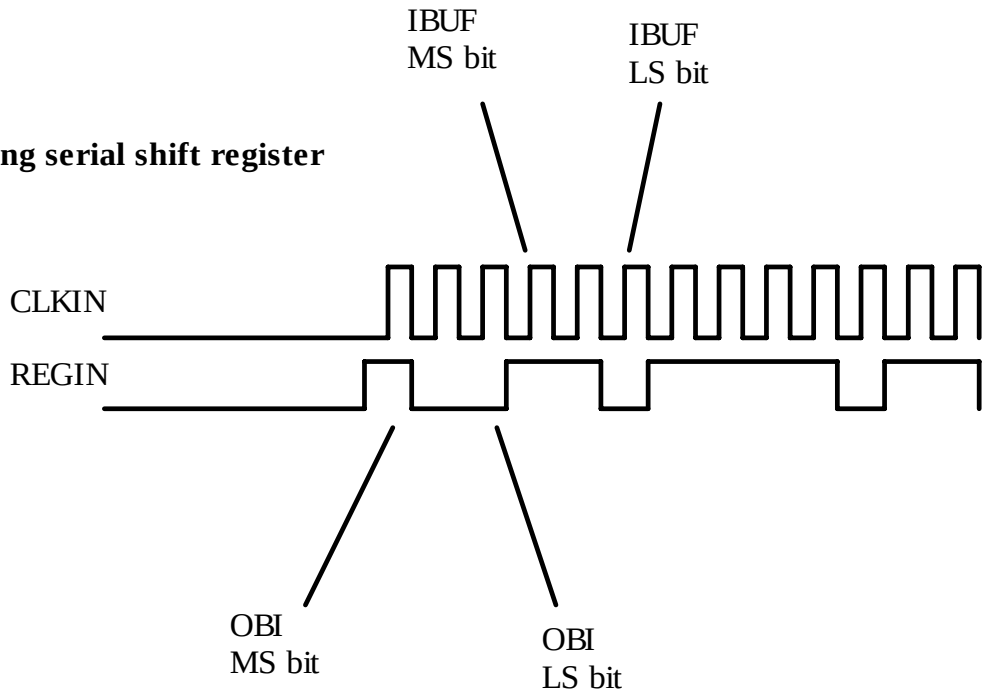
Loading sequence of VA1TA chips on ALPHA hybrid.

The first chip that is loaded chip ‘3’ on the VATAC screen (That is chip 4 on the hybrid). This is a P side chip. The chip load order is Chip 4,3,2,1 where 4 and 3 are P side and 2 and 1 are N side.



The diagram below shows the order of the bits as they are sent from the VATAC to the hybrid. (Note -There is some activity on the REGIN line before the clock begins but we believe that this is used internally in the VATAC since no clocks are issued to clock it into the VA1TA register.)

Loading serial shift register

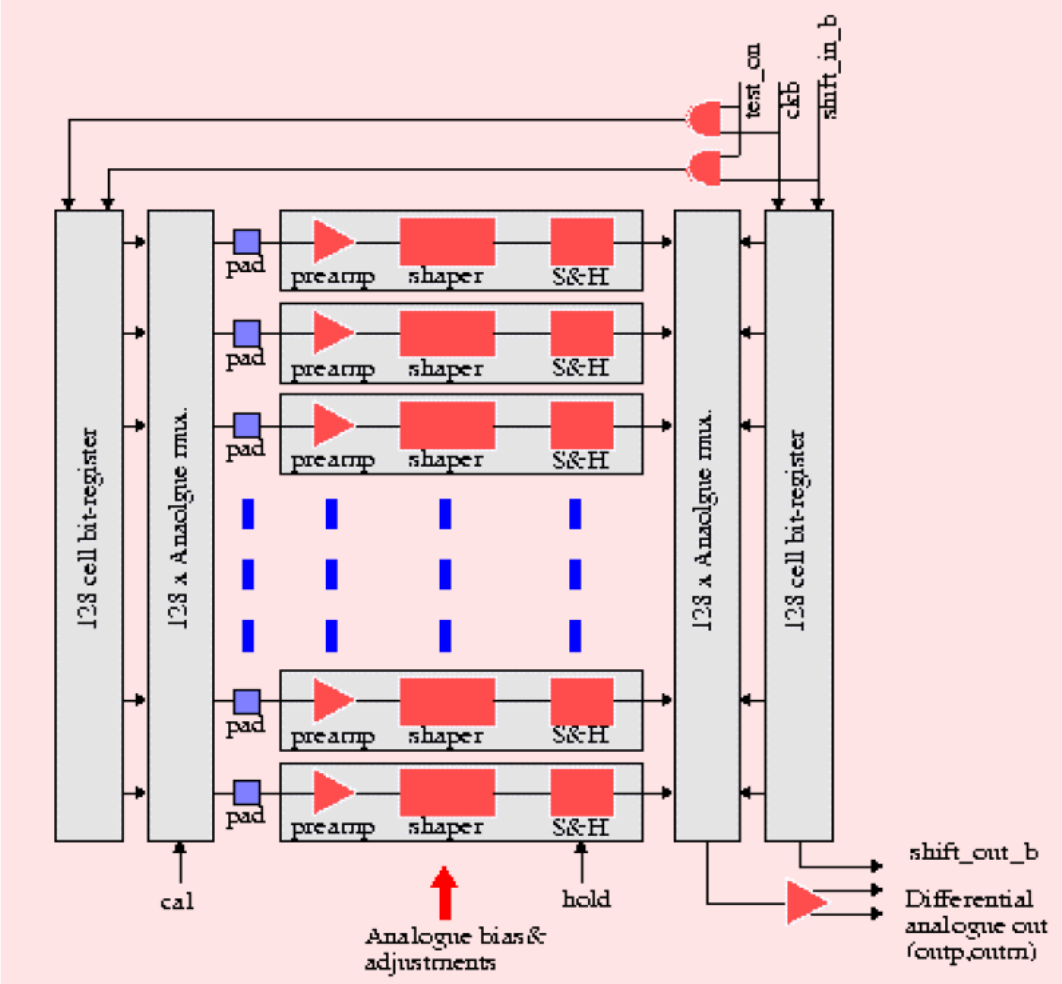


Bit 0 in the bit stream is OBI Most Significant bit.
Bit 2 in the stream is OBI Least significant.
This pattern continues.
Loading a value of 4 for OBI in the VATAC gives the stream as shown (first three bits).
The value of IBUF shown is 6.

There should be 2720 clocks issued to load the full 4 chips.
The clocks are on a 400us period.

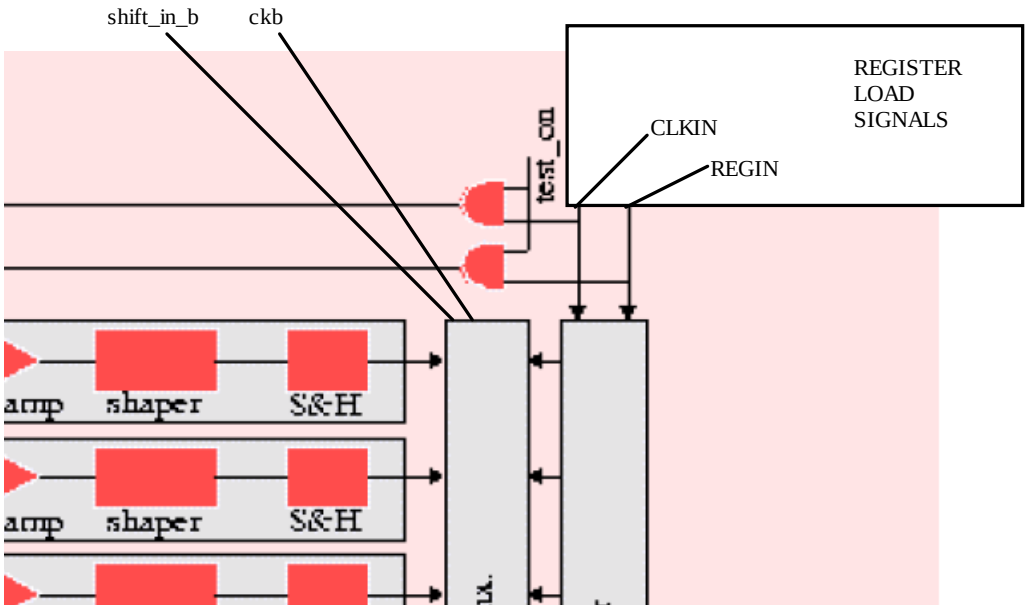
TEST PULSES

The VA1TA Manual has a diagram error in it. The following figure is incorrect.



The labels ckb and shift_in_b should be CLKIN (Register clock) and REGIN (Register data). The ckb and shift_in_b lines should go to the 128xAnalogue mux block in the diagram.
The LH register is the test register. The RH register is the channel enable register. All 128 channels are read out (even disabled channels) but only enabled channels will be part of the trigger OR.

The correct arrangement is shown below.



This explains the comment later in the VA1TA manual about the test register only being loaded when the test_on bit is set.

Quote. " ….In test mode, the *test_on* –bit must be set
(in addition to a bit in the *test enable* –register). The channel *disable* –register disables any channel with a high bit."

Additional readout information

DRESET

A DRESET signal is issued immediately after the hold is asserted in order to reset the output mux to be at channel zero for readout.