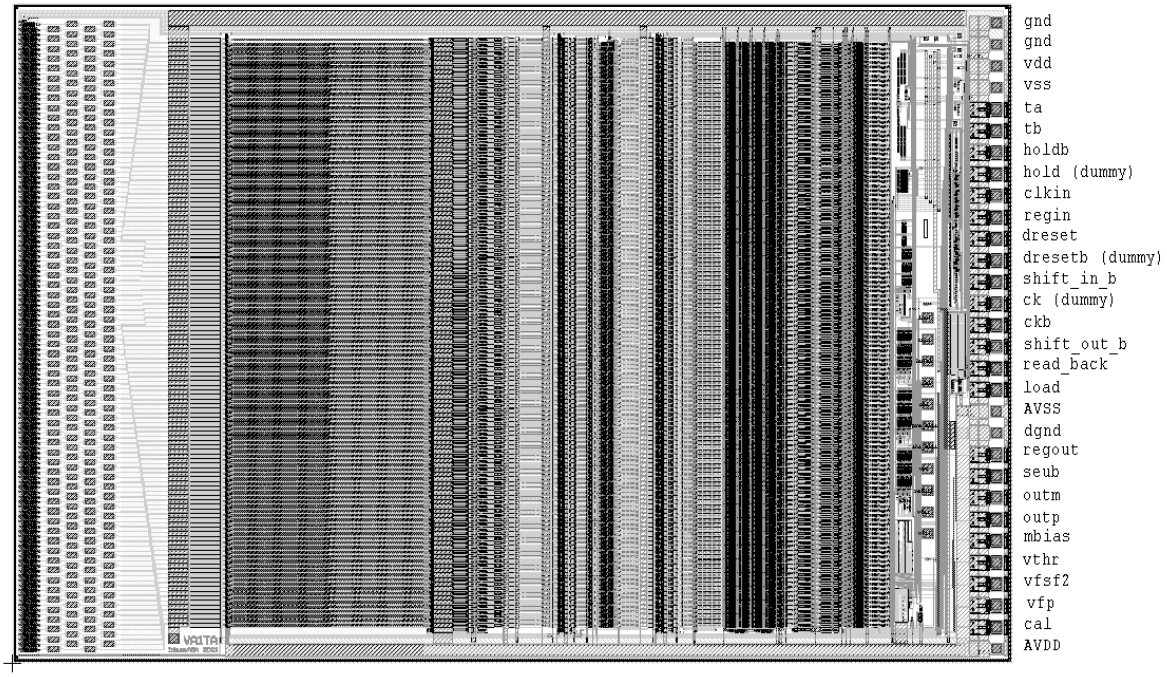
VA1TA

Version 0.9



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General

- Description:

  The Va1Ta is a radiation hard chip with 128 channels of low-noise/low-power charge sensitive preamplifier-shaper circuits, with simultaneous sample and hold, multiplexed analogue readout and calibration facilities. Current compensation is achieved by using a programmable sized resistor in the preamplifier feedback. Each channel also includes a fast-shaper, a discriminator and trigger logic. All channels share a common wire-or'ed trigger output. There is a 4 bits trim DAC in each channel to reduce threshold spread. All biases are generated internally from the externally applied current bias *mbias,* and can be adjusted by on-chip DACs. The flip-flops are implemented with error correction in order to improve SEU tolerance. Occurrence of SEU will be signalled on an external pad.

Physical

- Process: 0.35 µm N-well CMOS, double-poly, triple metal with epitaxial layer.
- Die size: 9.28 mm x 6.12 mm, thickness: ~ 725 µm
- Input bonding pads:
  Four rows. Normal connection to rows 1 and 2, redundant pads in rows 3 and 4.

  Pad size: 50 µm x 90 µm
  Pad pitch: 91.2 µm
  Row pitch: 170 µm (see. fig. 3&4)

- Output, control and power pads:
  Single row.
  Pad size: 90 µm x 90 µm
  Pad pitch: 200 µm (see fig. 3)

Electrical

All values are preliminary, and based on simulations. Verification with measurements has to be conducted.

Power rails: Vdd = +1.5V, Vss = -2.0V

Each with separate connections for analogue (avdd and avss) and digital sections (dvdd, dvss) of the chip.

Back contact: metalized, connect to avss (-2 V)

Current draw: Quiescent:

	Nominal:	Low:
dvdd:	16 mA	8 mA
dvss:	16 mA	8 mA
avdd:	16 mA	15 mA
avss:	- 60 mA	- 40 mA
gnd:	44 mA	25 mA

Input bias currents: All biases internally generated.

Peaking time:

Slow shaper:

Nominal: ~0.6 µs

Adjustable: ~ 0.3µs - 1µs

Fast shaper:

Switchable, 75ns/300ns

Power dissipation: Nominal values, quiescent:

195 mW

Low values, quiescent:

130 nW

ESD Protection:	Inputs:	None
	Control and other I/O:	Protection diodes to Vdd and Vss. ~300Ω series resistor except for *cal*, *mbias, vthr*, *outm* and *outp*.
Input stage:	Input device: PMOS referenced to gnd	
	Signal input potential: ~ -1.2 V to -1.3 V	
Gain:	The differential current gain on the outputs *outp* and *outm* is about ±10 µA/fC (at 1 Mip). The gain depends on setting parameters like VFS, Sha_bias etc.	
Linear range:	About ± 10 MIP (can handle both signal polarities) 20 MIP in single polarity can be used with adjustment of VREF	
Noise (ENC):	Typical values (to be measured):	
	180 + 7.5/pF e^-rms for 1 µsec peaking time	
Readout:	Controlled via 128-bit (output) shift register.	
	Analogue outputs (outp, outm) of two or more chips can be connected in parallel to drive the inputs of an external, differential, transimpedance amplifier. Max. read-out is 10 MHz, here care has to be taken not to load the output buffer with to high capacitance and resistance.	
Calibration/test:	Voltage step applied via external 1.8 pF capacitor to the cal-input. 2 mV step represents 1 MIP (=22400 e^- or 3.6 fC). Some additional noise has to be taken into account in test mode due to serial resistance and additional capacitance. Calibration signal can be given to one channel in a given chip at a time. The channel is selected via a 128-bit (input) shift register.	

Pad Description

The output, control and power pads of the *Va1Ta* are listed below from top to bottom. (see chip plot on next page (Fig. 1.).

Pad name	Type	Description	Nominal value
Gnd (2)	p	signal ground	0 V
Vdd	p	digital vdd	+1.5 V
Vss	p	digital vss	-2.0 V
ta	Do	Open drain trigger signal, positive part.	current
tb	do	Open drain trigger signal, negative part.	current
holdb	di	used to hold analogue data, see fig. 3.	Logical
dummy (hold)	di	*)	Logical
clkin	di	Clock for the digital serial shift register	Logical
regin	di	Input of the serial shift control register	Logical
Dreset	di	reset of digital part	Logical
dummy (dresetb)	di	*)	Logical
shift_in_b	di	start pulse for read-out	Logical
dummy (ck)	di	*)	Logical
Ckb	di	clock for read-out register, see fig. 3.	Logical
shift_out_b	do	Signalling end of read-out. Can be used as shift_in_b for next chip.	Logical
Read_back	Di	Control signal for reading back the value from the latches into the serial shift register.	Logical
load	di	Control signal for loading the latches in the serial shift register.	Logical
Avss	p	Analogue vss (+ chip backplane)	-2.0 V
Dgnd	p	signal ground, digital part	0 V
regout	do	Output of the serial shift control register	Logical
seub	do	Open drain pulse signal flagging that a SEU has occurred.	Current, Logical
outm	ao	Negative output signal (current)	
outp	ao	Positive output signal (current)	

mbias	ai	Reference bias for the main bias network. All other biases derived from this.	500 µA
vthr	Ai	Threshold voltage for discriminators. Internally generated.	5000 e^-
Vfsf2		Bias voltage for the feedback MOS in the fast shaper. Internally generated.	
vfp	ai	Control voltage to feedback resistance in pre-amplifier. Internally generated.	
cal	ai	Test input signal	1 MIP
avdd	p	Analogue vdd	+1.5 V

p = power, di = digital in, do = digital out, ai = analogue in, ao = analogue out

*) These 'dummy' signals are recommended for high performance. They should be used to add complementary signals to the effective ones in order to minimise digital signal-feed through to the analogue output.

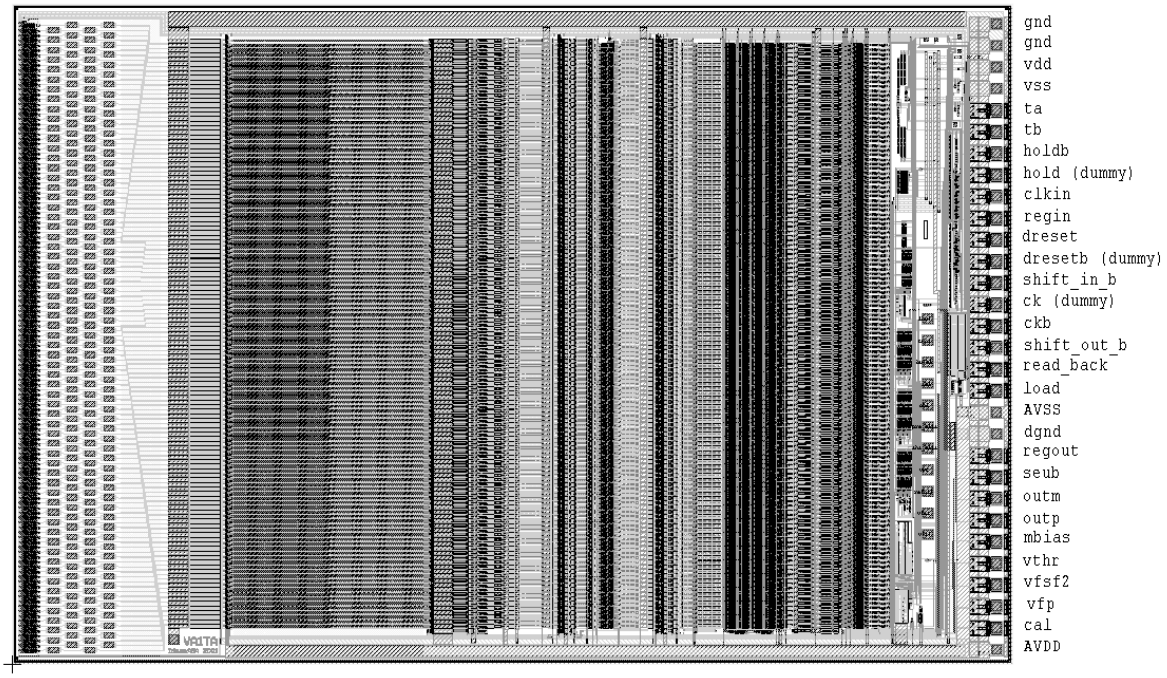

Fig. 1: The *VA1TA* circuit.

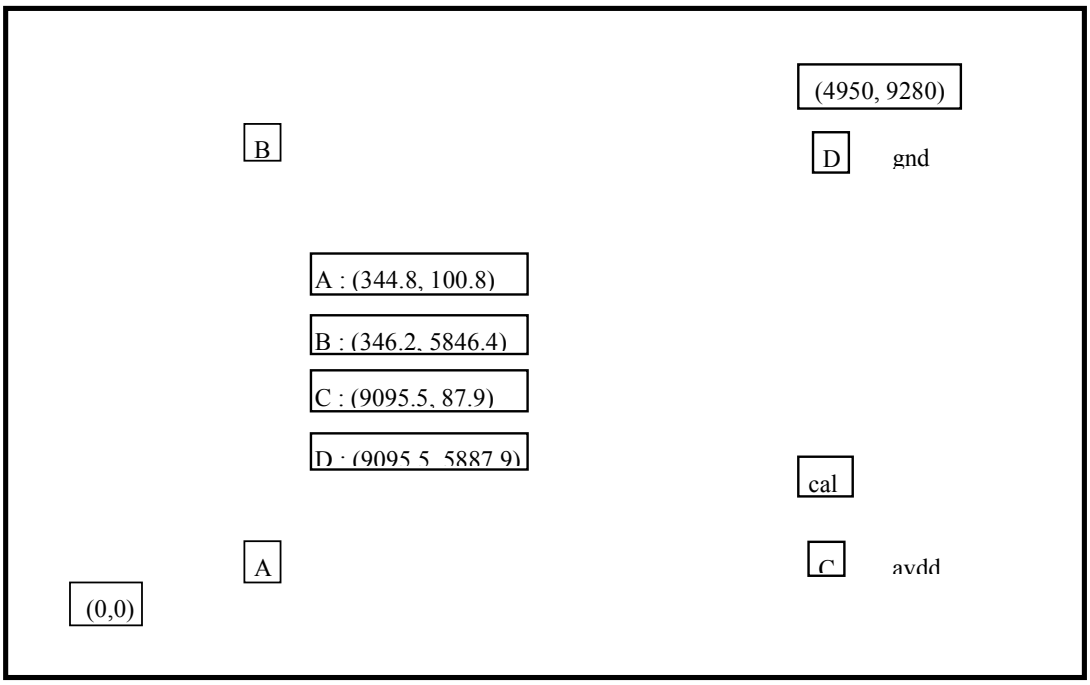

Fig. 2 Chip geometry & pad placement (Not to scale - all dimensions in µm. Please note that the referred co-ordinates are layout co-ordinates. Add 50-100 µm on each side for scribe/cutting tolerances).

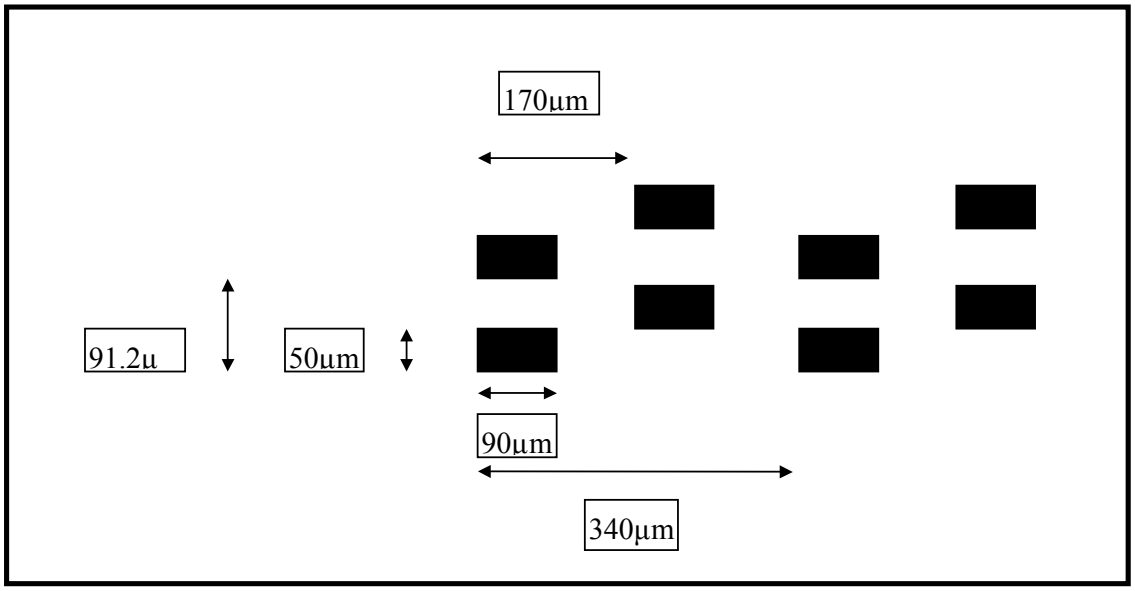

Fig. 3. Definition of input pad size and pitch

Functional Description

As shown in Fig. 4 the chip consists of 128 identical parallel charge sensitive amplifiers.

The output of all amplifiers enters corresponding inputs of a 128 channel multiplexer. The switches in the multiplexer are controlled by a bit-register which runs in parallel. The output of the mux goes directly out of the chip via the output buffer (signal = '**outp**' - '**outm**'). Only one of the switches in the mux can be ¨on ¨ at a time. That is one amplifier (channel) at a time can be seen on the output of the chip. The bit in the register ripples in sequence from the top- to the bottom- channel by clocking '**ckb**'. The clock can be stopped at any point which will leave the connection between the current channel and the output, which remains enabled.

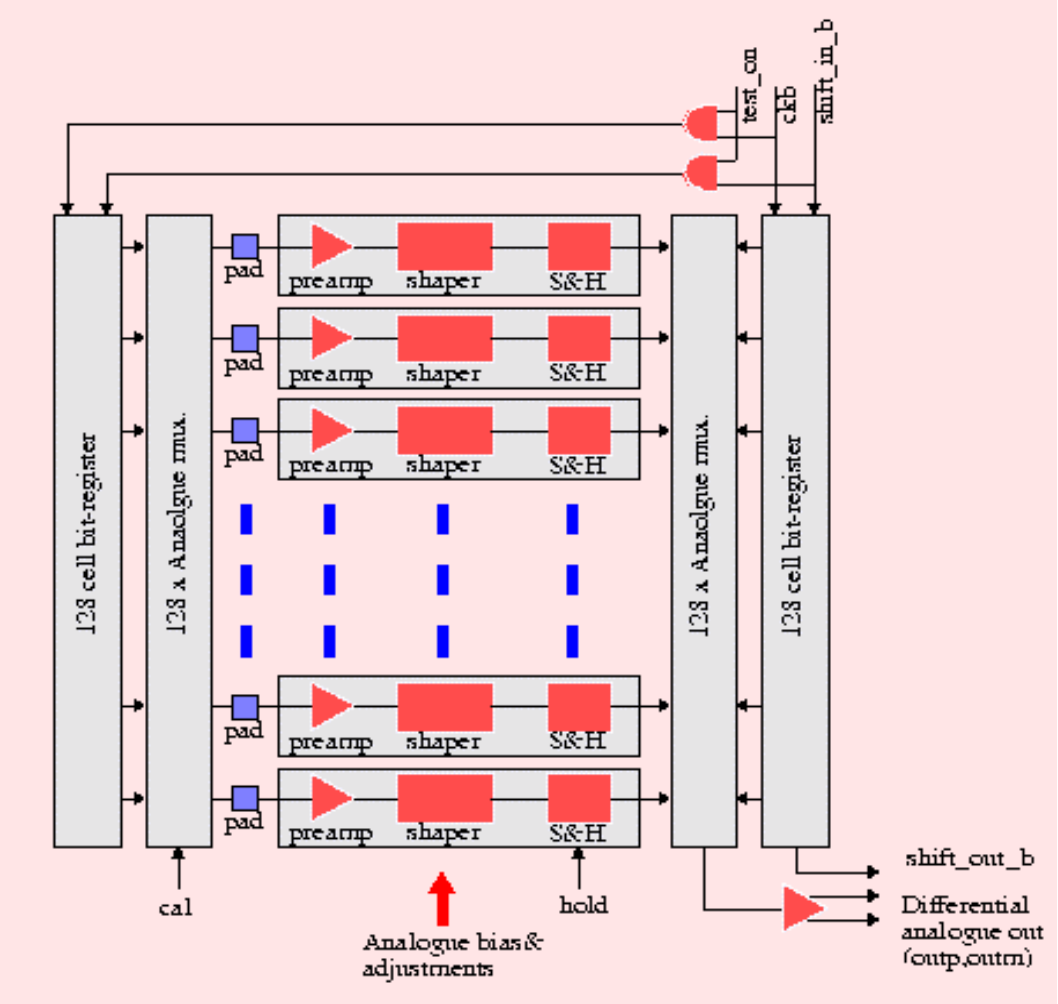

Fig 4. VA1TA Architecture, Va-part

The TA part is useful only together with the VA placed in the front. The concept is (see Fig.5) that TA and VA share the same preamplifier which is located on the VA the inputs of TA is directly coupled to corresponding outputs of these preamplifiers.

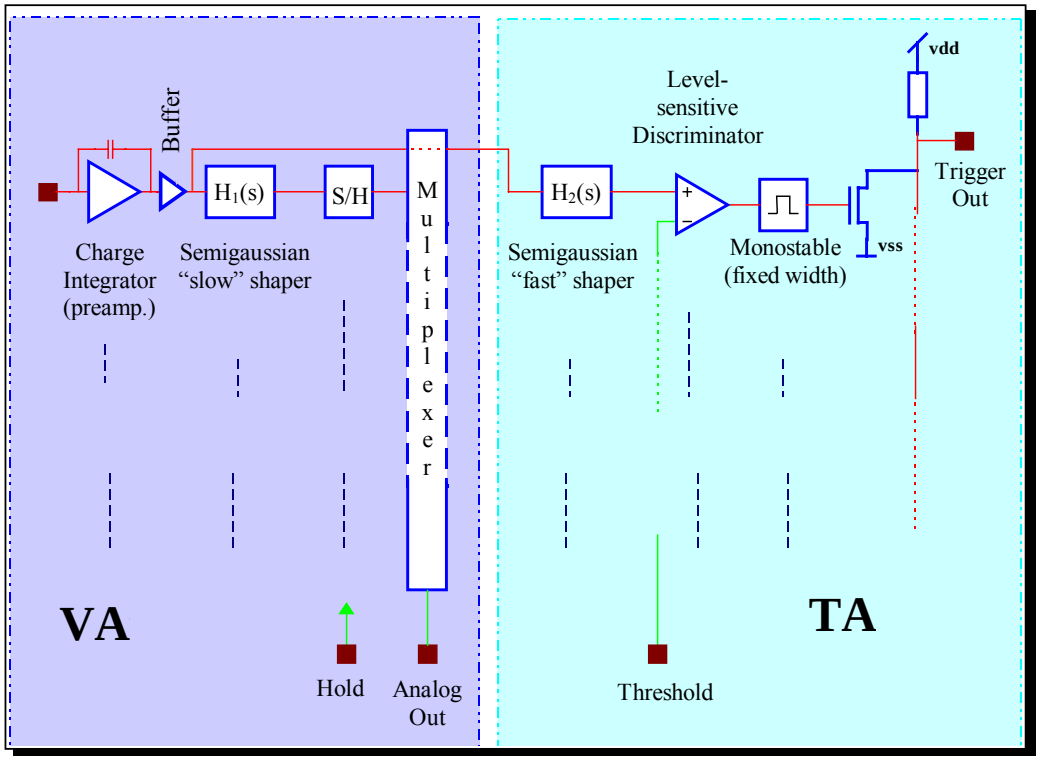

Fig 5. The VA-TA principle

As shown in Fig.6 the TA consists of 128 identical parallel channels. Each channel includes a fast CR-RC 75ns/300ns shaper followed by a level-sensitive discriminator. The discriminator is preceded by a High-Pass filter (not shown) with a very low cut-off frequency in order to reduce offset-spread across chip.

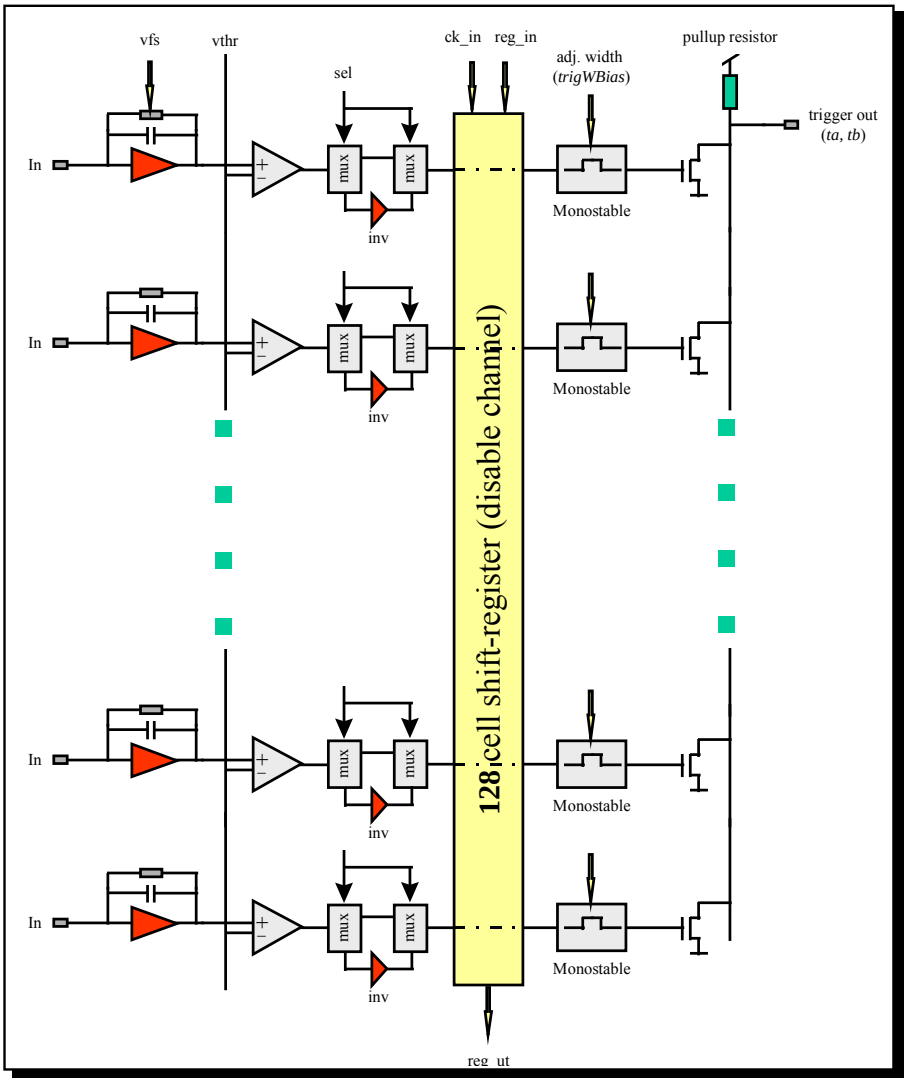

Fig 6. TA Architecture

Following the discriminator, which threshold is externally adjustable (***vthr***), is a circuitry which makes it possible to select between usage for positive or negative input signals.

Following this circuitry is an edge-trigged monostable flip-flop that gives a fixed pulse-width which is externally adjustable (***trigWbias***). At the end of the channel is a pull-down transistor that serves as one input to all 128 channels wire-or circuitry.

Whenever a signal in any of the channels is rising above the discriminator threshold the wire-or'ed output will cause a chip-global trigger output on $\mathbf{t_a}$ end $\mathbf{t_b}$.

Current compensation

Current compensation is achieved by placing a Nwell-resistor in parallel with the *Vfp*-transistor in the preamp feedback-loop. The two control signals *R1* and *R2* are used to choose the value of the Nwell-resistor (see table 1). The actual current sinking is done by the preamp. A sketch showing the principle is shown in figure 7.

R1	R2	Nwell resistor value
0	0	Shut off
1	0	2 MΩ
0	1	4 MΩ

Table 1: Nwell resistor value as a function of the control signals *R1* and *R2*.

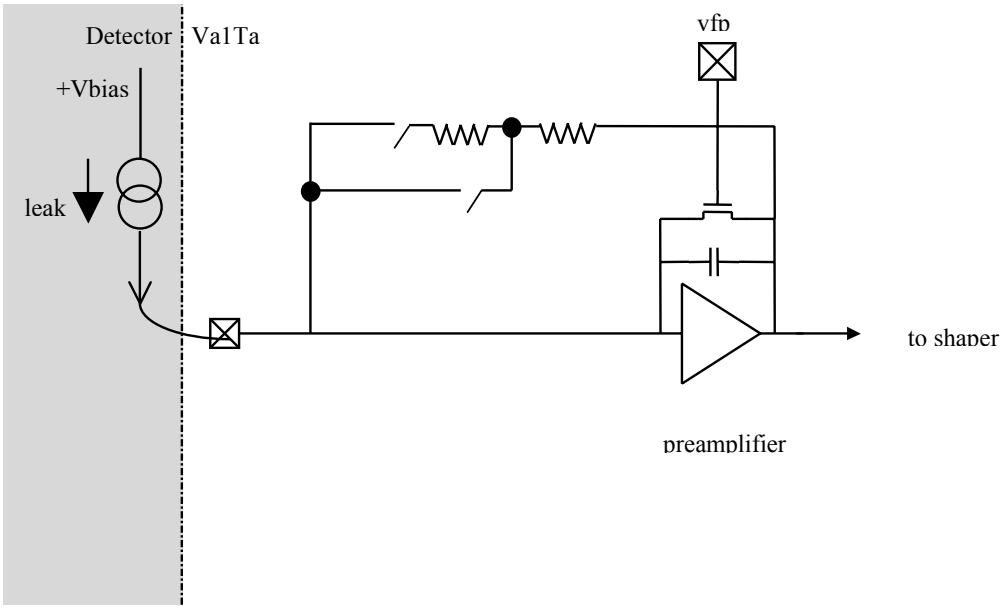

Fig. 7: Simplified schematic showing the current compensation employed in the *Va1Ta*. The switches are operated by *R1* and *R2*.

Serial shift register structure

The serial shift register used for slow control is implemented with flip-flops specially designed to be SEU tolerant. A schetch showing the principle of these cells is shown in figure 8. Bits are shifted into the cell through the *D* pin into the D-flip-flop by applying pulses at the external clock pad. The output of the DFF is shifted out through the *Q* output pin. When all bits have been shifted to the correct place in the serial shift register, a pulse should be applied to the *load* pin. This will open the latches, and store the value of the DFF in the three parallel latches. The stored values in the latches are seen by two different blocks of sequential logic. The *Majority selection module* outputs the logic value that the majority of the latches store. This logic value is the value that is actually used by the chip logic, and is output through the *valid bit* pin.

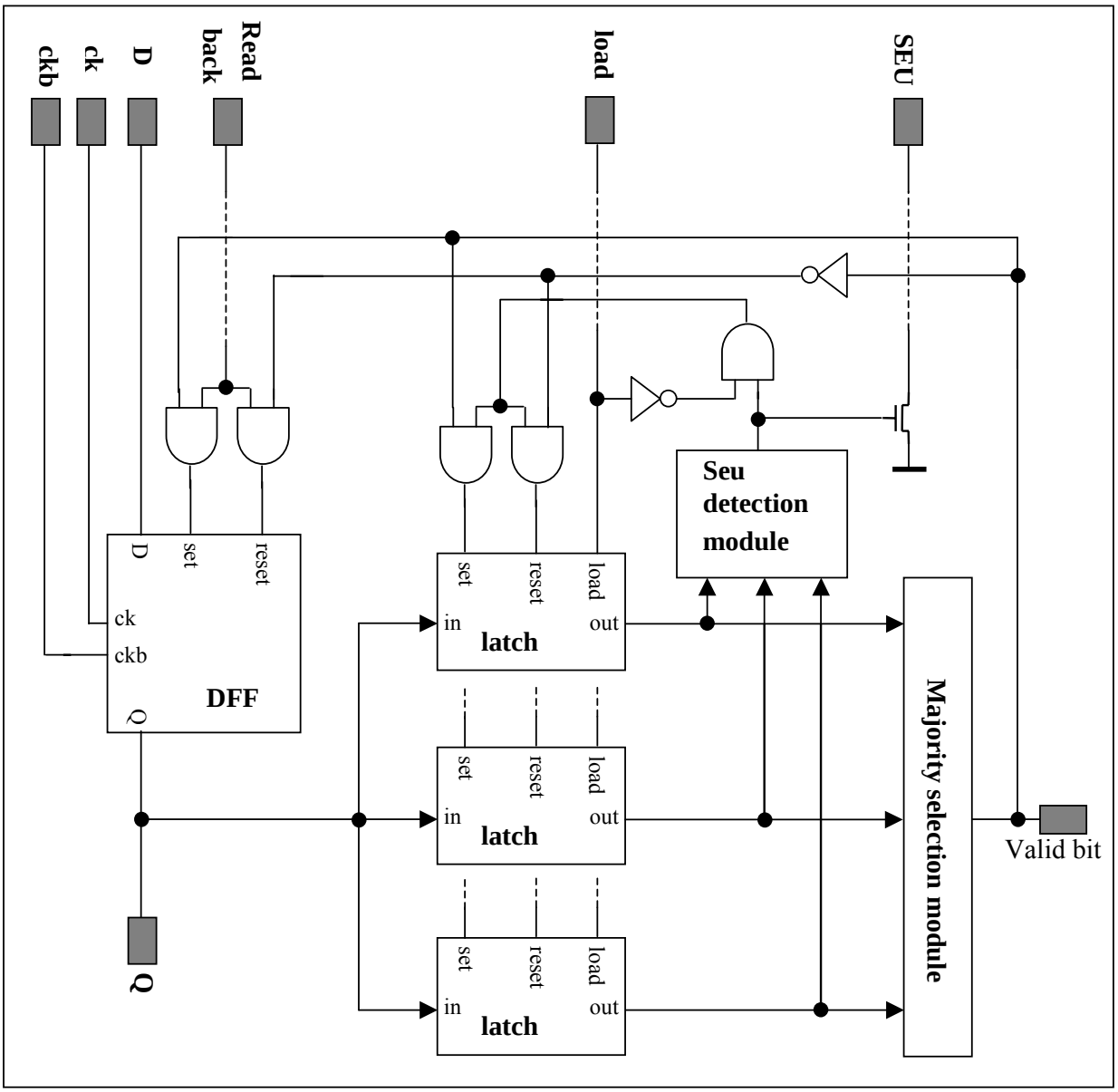

Fig. 8: Overview of the architecture of a SEU-flip-flop.

In this way, a SEU occurring in one of the three latches or in the DFF will not be visible to the chip logic because of the added redundancy. The *SEU detection module* outputs a logic high signal if a difference is detected between the three latch outputs. If a difference is detected, all three latches are corrected based on the valid bit value and the *set/reset* inputs in the latches. Note that the *load* signal is used to disable this feedback mechanism during initialisation of the latches.

In addition to the correction feedback to the latches, the output of the *SEU detection module* turns on a current source attached to the *SEU* pin. This line is wire-Or'ed with other SEU-flip-flops, and is connected to other modules on the chip that produces a defined output current pulse through the external pin *seu*.

The value stored in the latches can be read back into the DFF of the serial shift register by applying a pulse to the external *read_back* pad. This will force the DFF to the value of valid bit through a feedback mechanism connected to the set/reset inputs on the DFF.

Control register

The Va1Ta chip contains a 680 bits long shift register which can be loaded serially using *RegIn* (serial data) and *ClkIn* (clock). A more thorough description of the contents of the register is found below and in figure 9.

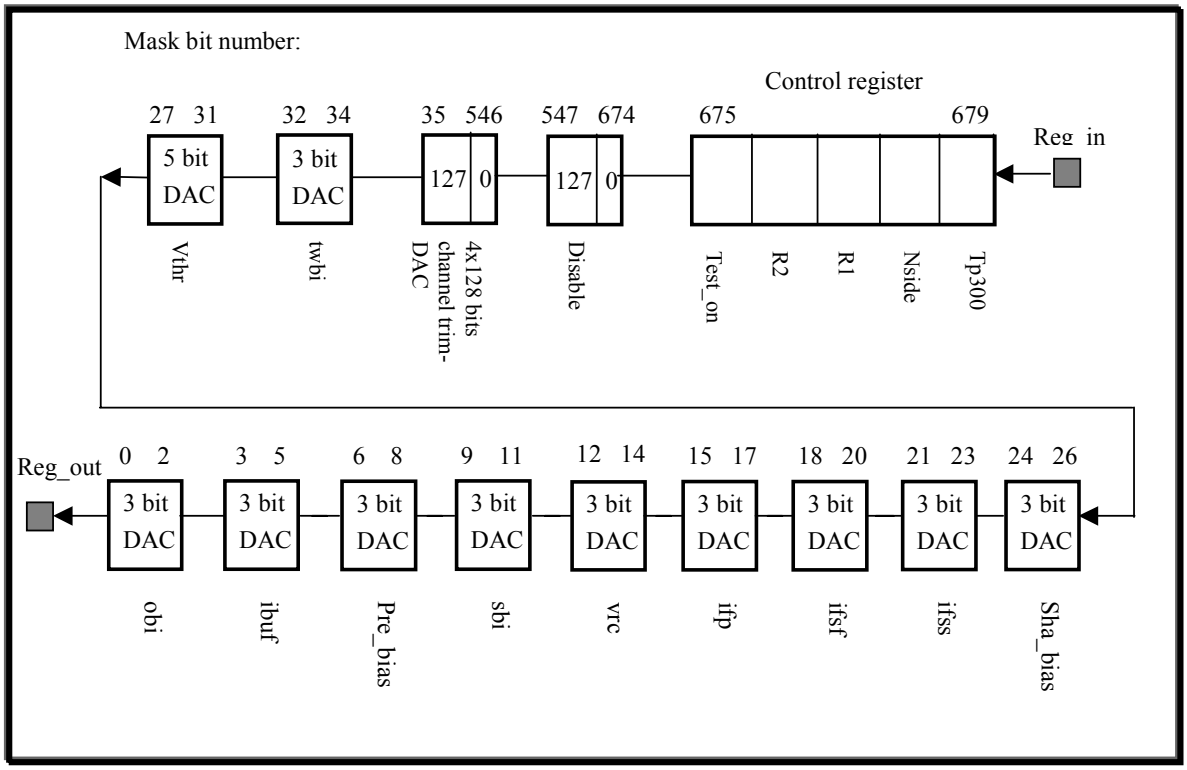

Figure 9: The sequence of the serial shift register mask. The sequence numbers are shown at the top of the boxes. Bit 0 is the first bit to be loaded. The channel numbers are indicated inside the boxes for the channel disable register and the channel threshold DAC register.

The serial shift register is shown in figure 9. The bits in the control register have the following function. A "1" in *Tp300* sets the peaking time of the fast shaper to 300ns. "0" sets the peaking time to be 75ns. A "1" in *nside* will prepare the channel for negative input signals. This control signal affects both bias generation and channel logic. The bits *R1* and *R2* controls the feedback resistor in the preamplifier, and are described in table 1. In test mode, the *test_on* –bit must be set (in addition to a bit in the *test enable* –register). The channel *disable* –register disables any channel with a high bit.

Each channel also includes a four bit DAC to trim the local threshold voltage. The first of the bits to be loaded into these DACs will be referred to as *bit1*. Table 2 shows the relation between DAC-bits and nominal threshold shift. The last of the channel registers, is the *test enable* –register. To test a channel through the *cal*-input, the channel's *test enable* bit must be set high in addition to the *test_on* –bit in the control register. The last 35 bits in the shift register consist of the 11 global bias DACs. The effect of the programming of the DACs is shown in table 3 to 10.

trigwbias:

This current bias adjusts the duration of the trigger (data output pulse width). *Trigwbias* has an internal DAC, Table 2 shows the programmable trigger width. This node is accessible through the external pad *trigwbias*. Current out of the chip decreases the trigger width. The nominal internally generated current is 3.25 μA.

Bit1	Bit2	Bit3	Trigger width (ns)
0	0	0	Default (105)
0	0	1	90
0	1	0	80
0	1	1	70
1	0	0	Default
1	0	1	125
1	1	0	150
1	1	1	200

Table 2: The relationship between the DAC bits and the trigger width.

Threshold DACs:

Adjust this voltage in order to set the threshold of all the 128 discriminators on the chip. Each channel has a separate DAC to tune the local threshold. In addition, there is a global DAC to give a on-chip global threshold voltage. Table 3 applies to the channel trim DACs, table 4 to the global threshold DAC. Be aware that if the netsum of the ± currents in the channel threshold trim DACs is non-zero, a common term offset will occur on the global threshold voltage.

Bit1	Bit2	Bit3	Bit4	Offset change (mV)
0	0	0	0	None
0	0	0	1	- 1
0	0	1	0	- 2
0	0	1	1	- 3
0	1	0	0	-4
0	1	0	1	-5
0	1	1	0	-6
0	1	1	1	-7
1	0	0	0	None
1	0	0	1	+ 1
1	0	1	0	+ 2
1	0	1	1	+ 3
1	1	0	0	+4
1	1	0	1	+5
1	1	1	0	+6
1	1	1	1	+7

Table 3: The relationship between the DAC bits and the resulting threshold voltage offset in the channels.

Bit1	Bit2	Bit3	Bit4	Bit5	Threshold (Equivalent input charge)
0	0	0	0	0	2000 e^-
0	0	0	0	1	2200 e^-
0	0	0	1	0	2400 e^-
0	0	0	1	1	2600 e^-
0	0	1	0	0	2800 e^-
0	0	1	0	1	3000 e^-
0	0	1	1	0	3200 e^-
0	0	1	1	1	3400 e^-
0	1	0	0	0	3600 e^-
0	1	0	0	1	3800 e^-
0	1	0	1	0	4000 e^-
0	1	0	1	1	4200 e^-
0	1	1	0	0	4400 e^-
0	1	1	0	1	4600 e^-
0	1	1	1	0	4800 e^-
0	1	1	1	1	5000 e^-
1	0	0	0	0	5200 e^-
1	0	0	0	1	5400 e^-
1	0	0	1	0	5600 e^-
1	0	0	1	1	5800 e^-
1	0	1	0	0	6000 e^-
1	0	1	0	1	6200 e^-
1	0	1	1	0	6400 e^-
1	0	1	1	1	6600 e^-
1	1	0	0	0	6800 e^-
1	1	0	0	1	7000 e^-
1	1	0	1	0	7200 e^-
1	1	0	1	1	7400 e^-
1	1	1	0	0	7600 e^-
1	1	1	0	1	7800 e^-
1	1	1	1	0	8000 e^-
1	1	1	1	1	8200 e^-

Table 4: The relationship between the DAC bits and the resulting on-chip global threshold.

Sha_bias:

This is the bias current for the slow shapers. The bias can be tuned by an internal DAC. Table 5 shows the relation between the shaper bias and the DAC bits. Current out of the chip decreases the bias value (nominal value 22 μA). The peaking time of the shaper (Tp) is determined by this bias together with the *ifs* –bias.

Bit1	Bit2	Bit3	Bias current (μA)
0	0	0	Default (22)
0	0	1	19
0	1	0	16
0	1	1	13
1	0	0	Default
1	0	1	25
1	1	0	28
1	1	1	31

Table 5: The relationship between the DAC bits and *shabias*.

The Ifss DAC:

DC current for controlling the slow shaper feedback resistance (NMOS device). The internally generated *ifs* should be approx. 75 nA, but will also be externally adjustable through the pad *ifs*. Current out of the chip decreases the bias value and increases the shaper feedback resistor. Table 6 shows the relation between the bias and the *ifs*-DAC bits.

Bit1	Bit2	Bit3	Bias current (nA)
0	0	0	Default (75)
0	0	1	55
0	1	0	35
0	1	1	15
1	0	0	Default
1	0	1	135
1	1	0	195
1	1	1	255

Table 6: The relationship between the DAC bits and the *ifs* -bias.

The Ifsf DAC:

DC current for controlling the shaper feedback resistance (NMOS device). The internally generated *ifs* is 45 nA or 3.9 µA, depending on the setting of the *tp300* bit. It is also externally adjustable through the pad *ifsf*. Current out of the chip decreases the bias value and increases the shaper feedback resistor. Table 7 and 8 shows the relation between the bias and the *ifsf*-DAC bits.

Bit1	Bit2	Bit3	Bias current (µA)
0	0	0	Default (3.9)
0	0	1	2.9
0	1	0	1.9
0	1	1	0.9
1	0	0	Default
1	0	1	8.9
1	1	0	13.9
1	1	1	18.9

Table 7: The relationship between the DAC bits and the *ifs* –bias with tp300 set to "0".

Bit1	Bit2	Bit3	Bias current (nA)
0	0	0	Default (45)
0	0	1	35
0	1	0	25
0	1	1	15
1	0	0	Default
1	0	1	70
1	1	0	95
1	1	1	120

Table 8: The relationship between the DAC bits and the *ifs* –bias with tp300 set to "1".

The Ifp DAC:

DC current for controlling the preamp feedback resistance (NMOS device). The internally generated *ifp* should be approx. 0.7 nA. This bias is turned off in case the *R1*/*R2* option is used. Table 9 shows the relation between the *ifp* bias and the DAC bits.

Bit1	Bit2	Bit3	Trigger width (nA)
0	0	0	Default (0.7)
0	0	1	0.5
0	1	0	0.3
0	1	1	0.1
1	0	0	Default
1	0	1	3.7
1	1	0	6.7
1	1	1	9.7

Table 9: The relationship between the DAC bits and the *ifp* -bias.

vrc:

This is the bias current for the high-pass filter in front of the discriminators. The bias is generated internally. This bias can be tuned by an internal DAC. Table 10 and 11 show the relation between the vrc bias and the DAC bits. The nominal value depends on the setting of the negpol bit. If the bit is set low, the default is 1.1 µA, otherwise 250nA.

Bit1	Bit2	Bit3	Bias current (µA)
0	0	0	Default (1.1)
0	0	1	0.8
0	1	0	0.5
0	1	1	0.2
1	0	0	Default
1	0	1	1.5
1	1	0	1.9
1	1	1	2.3

Table 10: The relationship between the DAC bits and *shabias* with the *negpol* bit set to "0".

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Bit1	Bit2	Bit3	Bias current (nA)
0	0	0	Default (250)
0	0	1	200
0	1	0	150
0	1	1	100
1	0	0	Default
1	0	1	500
1	1	0	750
1	1	1	1000

Table 11: The relationship between the DAC bits and *shabias* with the *negpol* bit set to "1".

sbi:

This is the bias current for the fast shapers. The nominal bias is generated internally, but can be tuned by an internal DAC. Table 12 shows the relation between the fast shaper bias and the DAC bits. Current out of the chip decreases the bias value (nominal value 70 μA). The peaking time of the fast shaper (Tp) is determined by this bias together with the *ifsf* –bias.

Bit1	Bit2	Bit3	Bias current (μA)
0	0	0	Default (70)
0	0	1	60
0	1	0	50
0	1	1	40
1	0	0	Default
1	0	1	80
1	1	0	90
1	1	1	100

Table 12: The relationship between the DAC bits and *sbi*.

Pre_bias:

This is the bias current for the preamplifiers. The nominal bias is generated internally, but can be tuned by an internal DAC. Table 13 shows the relation between the shaper bias and the DAC bits. Current out of the chip decreases the bias value (nominal value 300 µA).

Bit1	Bit2	Bit3	Bias current (µA)
0	0	0	Default (300)
0	0	1	250
0	1	0	200
0	1	1	150
1	0	0	Default
1	0	1	350
1	1	0	400
1	1	1	450

Table 13: The relationship between the DAC bits and *shabias*.

ibuf:

This is the bias current for the serial analog output buffer. The nominal bias is generated internally, but can be tuned by an internal DAC. Table 14 shows the relation between the buffer bias and the DAC bits. Current out of the chip decreases the bias value (nominal value 180 µA). The linear range and gain may be tuned with this bias. 220 µA is the recommended value for use.

Bit1	Bit2	Bit3	Bias current (µA)
0	0	0	Default (180)
0	0	1	160
0	1	0	140
0	1	1	120
1	0	0	Default
1	0	1	200
1	1	0	220
1	1	1	240

Table 14: The relationship between the DAC bits and *ibuf*.

obi:

This is the bias current for the discriminators. The nominal bias is generated internally, but can be tuned by an internal DAC. Table 15 shows the relation between the discriminator bias and the DAC bits. Current out of the chip decreases the bias value (nominal value 90 µA).

Bit1	Bit2	Bit3	Bias current (µA)
0	0	0	Default (90)
0	0	1	80
0	1	0	70
0	1	1	60
1	0	0	Default
1	0	1	100
1	1	0	110
1	1	1	120

Table 7: The relationship between the DAC bits and *shabias*.

Bias connections to the chip

The only bias that has to be connected is the *mbias*. All other biases are internally generated. However, *ifss, ifsf,* and *vthr* are available through external pads.

Other signals

cal is connected directly to the test register. When desired, set the chip in test-mode, select a channel (see earlier) and apply a proper voltage step on *cal* to emulate a charge input signal in one channel (only one at a time).

ClkIn and *RegIn* are the clock and input for the shift register respectively. Logic values. Data at *RegIn* is sampled by the clock on the falling edge. The rise and fall time of the clock should not exceed 100ns. For daisy-chaining of chips, *RegIn* should only be connected to the first chip in the chain. For the others, *RegIn* should be fed from *RegOut* of the previous chip. There are three more external pads that are related to the operation of the control register, all of them part of the SEU flip-flop operation. *Read_back* is used for reading back the contents of the latches into the shift-register. *Load* is used to copy the contents of the serial shift register into the latches. Both signals are active high and level sensitive. They should be pulsed when operated. Their function is more thoroughly discussed in the section about the serial shift register. *seu* is the output flag for all of the SEU flip-flops. Whenever a SEU is detected in the shift register, an open drain current pulse (direction into the chip) will appear on this pin. The pulse width will be approximately 1µs.

Normal mode of operation

The normal mode of operation is that the 128 inputs are connected to a detector from where the charge signal comes. After the physics event, each channel will integrate its eventual signal for 1µs. Usually, after the peak is reached (1µs), an external '**holdb**' signal should be applied to sample the value. Immediately after this a sequential read-out can be performed by activating the output bit-register using '**shift_in_b**' and '**ckb**'. See fig. 8 for an example of the timing in this mode. The logic part of the chip can be reset either by applying the '**dreset**' or, simply by running through a normal read-out once.

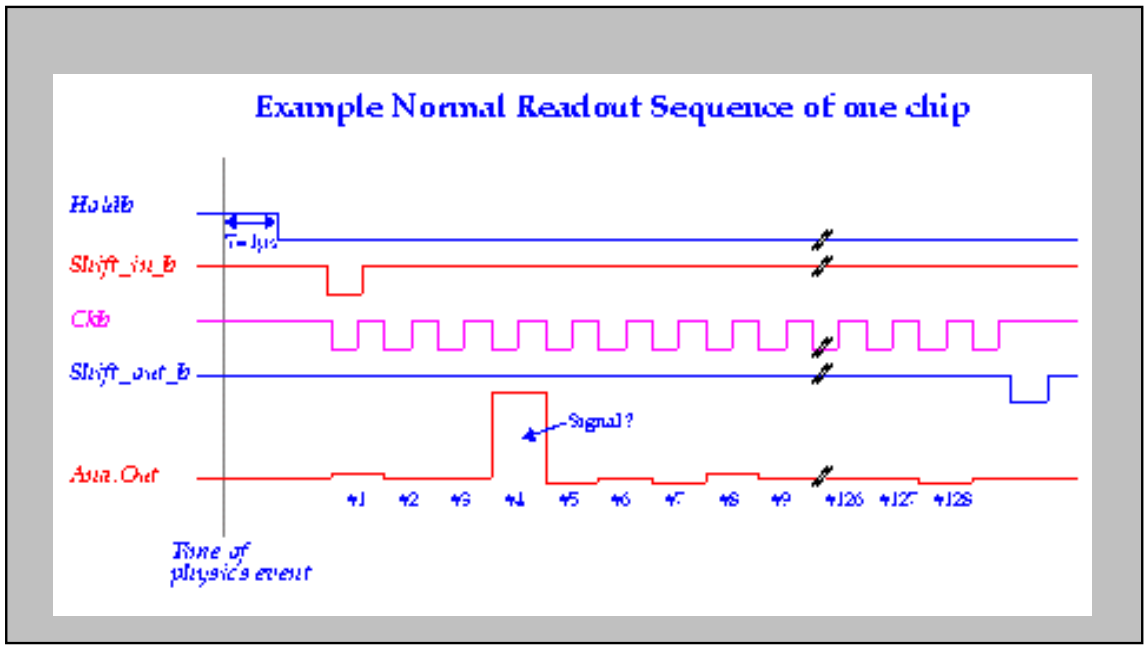
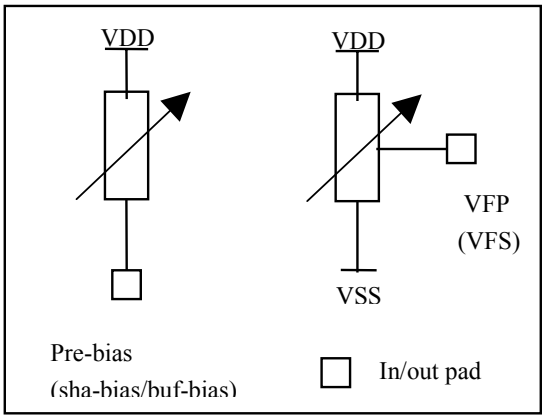


Fig 10. Read-out timing of VA1TA

Operation in test mode

Each of the inputs of the amplifiers can be accessed via the input pads on the left side, see Fig. 5. In test mode, it is not necessary to connect any of these. Instead, the test facility of the chip can be turned on ('**test-on**'). This will enable another mux./bit-register on the input to run exactly in parallel with the output mux./bit-register. This input mux. connects all the inputs to the '**cal**' pad via a switch controlled by the bit-register. Also, in this case, only one connection at a time is possible and this connection will always correspond to the same channel as is connected in the output mux.

Bias current generation



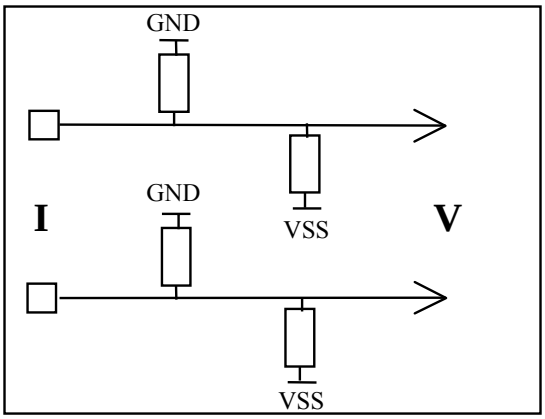


Fig 11. Bias current & Voltage generation

Fig 12. Analogue-Out termination (1 kOhm recommended)