ALPHA TTC Test VME Registers

These registers are for testing purposes some will change in the released code.

A32 –Address Space

XX000000: Run Mode register – 8 bits (Reset 0x00) (Read/Write)
- Bit 7: VA1TA Control Register Load
- Bit 6: VA1TA Control Register Read
- Bit 5: ADC Readout Step Mode = 1, ADC Readout Full Cycle 0
- Bit 4: Reserved
- Bit 3: Reserved
- Bit 2: Reserved
- Bit 1: VME Calibration Pulse = 0, Auto Generated Calibration Pulse = 1
- Bit 0: Internal Calibration Pulse 1, External Calibration Pulse 0

XX000001: TTC Status Register – 8 bits (Read Only)
- Bit 0: VA1 Control Shiftout BusyN
- Bit 1: FEC Readout BusyN

XX000002: FEC Address Register – 6 bits (Reset 0x00) (Read/Write)

XX000003: Command Register – 8 bits (Write Only)

Command:
- 0x0A – Calibration Pulse
- 0x09 – Step ADC Readout Clock
- 0x08 – Reset VA1TA Readout
- 0x07 – Read VA1TA Control Register
- 0x06 - Write VA1TA Control Register
- 0x05 – VA1 Readout Start

XX000004: ADC Trigger Delay – 8bits (Reset 0x00) (Read/Write)

50ns steps
0x01 : 95ns
0x02 : 145ns
.
0xFF : 12795ns
0x00 : 12845ns

XX000005: VETO Delay (VA1 Readout Delay) – 8bits (Reset 0x00) (Read/Write)

200ns steps
0x01 : 850ns
0x02 : 1050ns
.
0xFF : 51650ns

0x00 : 51850ns

XX000006: DAC B Data – 8bits (Reset 0x00) (Read/Write)
0x00 : 2.7mV
0x10 : 22.66mV
0x20 : 47.5mV
0x40 : 97.5mV
0x60 : 148.5mV
0x80 : 198.5mV

XX000007: DAC A Data – 8bits (Reset 0x00) (Read/Write)
0x00 : 2.7mV
0x10 : 22.66mV
0x20 : 47.5mV
0x40 : 97.5mV
0x60 : 148.5mV
0x80 : 198.5mV

XX000100 – **XX000154**: VA1TA Chip0 Control Register Bits (D32) (Read/Write)
LSB MSB

XX000100 … 32bits
XX000104 … 32bits
.
.
.
XX00014C … 32bits
XX000150 … 32bits

XX000154 … 8bits (Still written D32 cycle)

XX000180 – **XX0001D4**: VA1TA Chip1 Control Register Bits (D32) (Read/Write)
XX000200 – **XX000254**: VA1TA Chip2 Control Register Bits (D32) (Read/Write)
XX000280 – **XX0002D4**: VA1TA Chip3 Control Register Bits (D32) (Read/Write)

XX000300 – **XX000354**: VA1TA Chip0 Control Register Bits (D32) (Read/Write)
XX000380 – **XX0003D4**: VA1TA Chip1 Control Register Bits (D32) (Read/Write)
XX000400 – **XX000454**: VA1TA Chip2 Control Register Bits (D32) (Read/Write)
XX000480 – **XX0004D4**: VA1TA Chip3 Control Register Bits (D32) (Read/Write)

Instructions For Modes of Operations (Testing Modes)

For ADC clock stepping and VME Generated Calibration Pulse write:

- 0x21 to Run Mode Register (XX000000)

For the Command Register:

- Write 0x05 to start the ADC Readout (XX000003)
- Write 0x09 to step the ADC clock (XX000003)
- Write 0x0A to send 10us calibration pulse (XX000003) (set calibration values in DACa **(**XX000007) or DACb (XX000006) Data Registers first)

For ADC clock stepping and Auto Generated Calibration pulse write:

- 0x23 to Run Mode register (XX000000)

Calibration Pulse 1kHz/10us wide. (set calibration amplitude values in DACa (XX000007) or DACb (XX000006) Data Registers)

For the Command Register:

- Write 0x05 to start the ADC Readout (XX000003)
- Write 0x09 to step the ADC clock (one at a time 128 clocks + ½ clock at the end) (XX000003)

For "VETO" Mode

- Write 0x00 to Run Mode register (XX000000)

Calibration Pulse and ADC readout are generated by an external NIM pulse into VETO IN Lemo.