CPU
T2K FEB_Rev2 - Slow Control.SCHDOC

MSCB_RS485A, MSCB_RS485B
SMB_CLK, SMB_DAT
EN_BIASn[7..0], Backplane_Add[7..0]
BiasCurrentSense, BiasVoltageReadback
+6V_Analog_VMon, -6V_Analog_VMon, +6V_Dig_VMon, +6V_Analog_IMon, -6V_Analog_IMon, +6V_Dig_IMon
REG_Enable

SPI_MOSI, SPI_SCK, APD_DAC_CSn[7..0], SUM_DAC_CSn, DAC_ResetN
REG_Enable
CHG_PMP_CLK
ASUM_SYNC, ASUM_PdwnN, ASUM_TESTn
Da[8..1], Db[8..1]
JTAG_TCK, JTAG_TMS, CPU_TDO, XILINX_TDO, JTAG_TDI

SCA_ADC
T2K FEB_Rev2 - 50MSPS ADC.SCHDOC

ADC_DTP, ADC_PDWN
SCA1_VOUT_P, SCA1_VOUT_N
SCA2_VOUT_P, SCA2_VOUT_N

LVDS_ADC_CLK_P, LVDS_ADC_CLK_N, LVDS_ADC_DCO_P, LVDS_ADC_DCO_N, LVDS_ADC_FCO_P, LVDS_ADC_FCO_N, LVDS_ADC_DATA0_P, LVDS_ADC_DATA0_N, LVDS_ADC_DATA3_P, LVDS_ADC_DATA3_N

SCA
T2K FEB_Rev2 - SCA Interface.SCHDOC

SCA1_VOUT_P, SCA1_VOUT_N
SCA2_VOUT_P, SCA2_VOUT_N
LVDS_TRIG_P, LVDS_TRIG_N
APD_HATIN[63..0], APD_LATIN[63..0]
ASUM_OUT[7..0]

SCA1_Sc_ck, SCA1_Sc_en, SCA1_Sc_din, SCA1_Sc_dout
SCA2_Sc_ck, SCA2_Sc_en, SCA2_Sc_din, SCA2_Sc_dout
LVDS_SCA_WCK_P, LVDS_SCA_WCK_N, LVDS_SCA_RCK_P, LVDS_SCA_RCK_N, LVDS_SCA_READ_P, LVDS_SCA_READ_N, LVDS_SCA_WRITE_P, LVDS_SCA_WRITE_N

Backplane
T2K FEB_Rev2 - Backplane Connections.SCHDOC

LVDS_ADC_CLK_P, LVDS_ADC_CLK_N, LVDS_ADC_DCO_P, LVDS_ADC_DCO_N, LVDS_ADC_FCO_P, LVDS_ADC_FCO_N, LVDS_ADC_DATA0_P, LVDS_ADC_DATA0_N, LVDS_ADC_DATA3_P, LVDS_ADC_DATA3_N
SCA_SlowCnt_SCK0, SCA_SlowCnt_CS0, SCA_SlowCnt_MOSI0, SCA_SlowCnt_MISO0
SCA_SlowCnt_SCK1, SCA_SlowCnt_CS1, SCA_SlowCnt_MOSI1, SCA_SlowCnt_MISO1
LVDS_SCA_WCK_P, LVDS_SCA_WCK_N, LVDS_SCA_RCK_P, LVDS_SCA_RCK_N, LVDS_SCA_READ_P, LVDS_SCA_READ_N, LVDS_SCA_WRITE_P, LVDS_SCA_WRITE_N
AN_+6V_IN, AN_-6V_IN, DIG_+6V_IN, SLO_+5V
APDa[63..0], APDk[63..0]

Db[8..1], Da[8..1]
ASUM_CLK_P, ASUM_CLK_N
ADC_DTP, ADC_PDWN
LVDS_TRIG_P, LVDS_TRIG_N
LVDS_ASum_P, LVDS_ASum_N
MSCB_RS485A, MSCB_RS485B
BP_TCK, BP_TMS, BP_TDO, BP_TDI
JTAG_TCK, JTAG_TMS, XILINX_TDO, JTAG_TDI
AN_+6V_IN, AN_-6V_IN, DIG_+6V_IN, SLO_+5V
Backplane_Add[7..0]

APD_DAC
T2K FEB_Rev2 - 64 Channel Bias Control.SCHDOC

APD_DAC_CSn[7..0], SPI_SCK, SPI_MOSI, DAC_ResetN
APD_DAC_CSn[7..0], APD_DAC_SCK, APD_DAC_DIN, DAC_ResetN
APD_DAC[63..0]

BIAS_OUT
T2K FEB_Rev2 - BIAS Output.SchDoc

EN_BIASn[7..0], SMB_CLK, SMB_DAT, VREF_2.5V
EN_BIASn[7..0], SMB_CLK, SMB_DAT, VREF_2.5V, BIAS
BIAS_OUT[7..0], BIAS

CHRG_PUMP
T2K FEB_Rev2 - 80 Volt Charge Pump.SCHDOC

CHG_PMP_CLK, SMB_CLK, SMB_DAT, VREF_2.5V
CHG_PMP_CLK, SMB_CLK, SMB_DAT, VREF_2.5V, BIAS, BiasCurrentSense, BiasVoltageReadback
BIAS, BiasCurrentSense, BiasVoltageReadback

APD_INPUTS
T2K FEB_Rev2 - APD Inputs.SchDoc

APDk[63..0], BIAS_OUT[7..0]
APDk[63..0], BIAS_OUT[7..0], APD_HATIN[63..0], APD_LATIN[63..0], ASUM_IN[7..0]
APD_HATIN[63..0], APD_LATIN[63..0], ASUM_IN[7..0]

APD_SUM
T2K FEB_Rev2 - APD SUM.SCHDOC

ASUM_IN[7..0], SUM_DAC_CSn, SPI_SCK, SPI_MOSI, DAC_ResetN
ASUM_IN[7..0], SUM_DAC_CSn, SUM_DAC_SCK, SUM_DAC_DIN, SUM_DAC_CLRn, ASUM_CLK_P, ASUM_CLK_N, ASUM_SYNC, ASUM_PdwnN, ASUM_TESTn
ASUM_OUT[7..0], LVDS_ASum_P, LVDS_ASum_N, JTAG_TCK, JTAG_TMS, XILINX_TDI, XILINX_TDO
ASUM_OUT[7..0], LVDS_ASum_P, LVDS_ASum_N, JTAG_TCK, JTAG_TMS, CPU_TDO, XILINX_TDO

REGULATORS
T2K FEB_Rev2- Regulators.SCHDOC

AN_+6V_IN, AN_-6V_IN, DIG_+6V_IN, SLO_+5V, VREF_2.5V, REG_Enable
AN_+6V_IN, AN_-6V_IN, DIG_+6V_IN, SLO_+5V, VREF_2.5V, REG_Enable, +6V_Analog_VMon, -6V_Analog_VMon, +6V_Dig_VMon, +6V_Analog_IMon, -6V_Analog_IMon, +6V_Dig_IMon
+6V_Analog_VMon, -6V_Analog_VMon, +6V_Dig_VMon, +6V_Analog_IMon, -6V_Analog_IMon, +6V_Dig_IMon

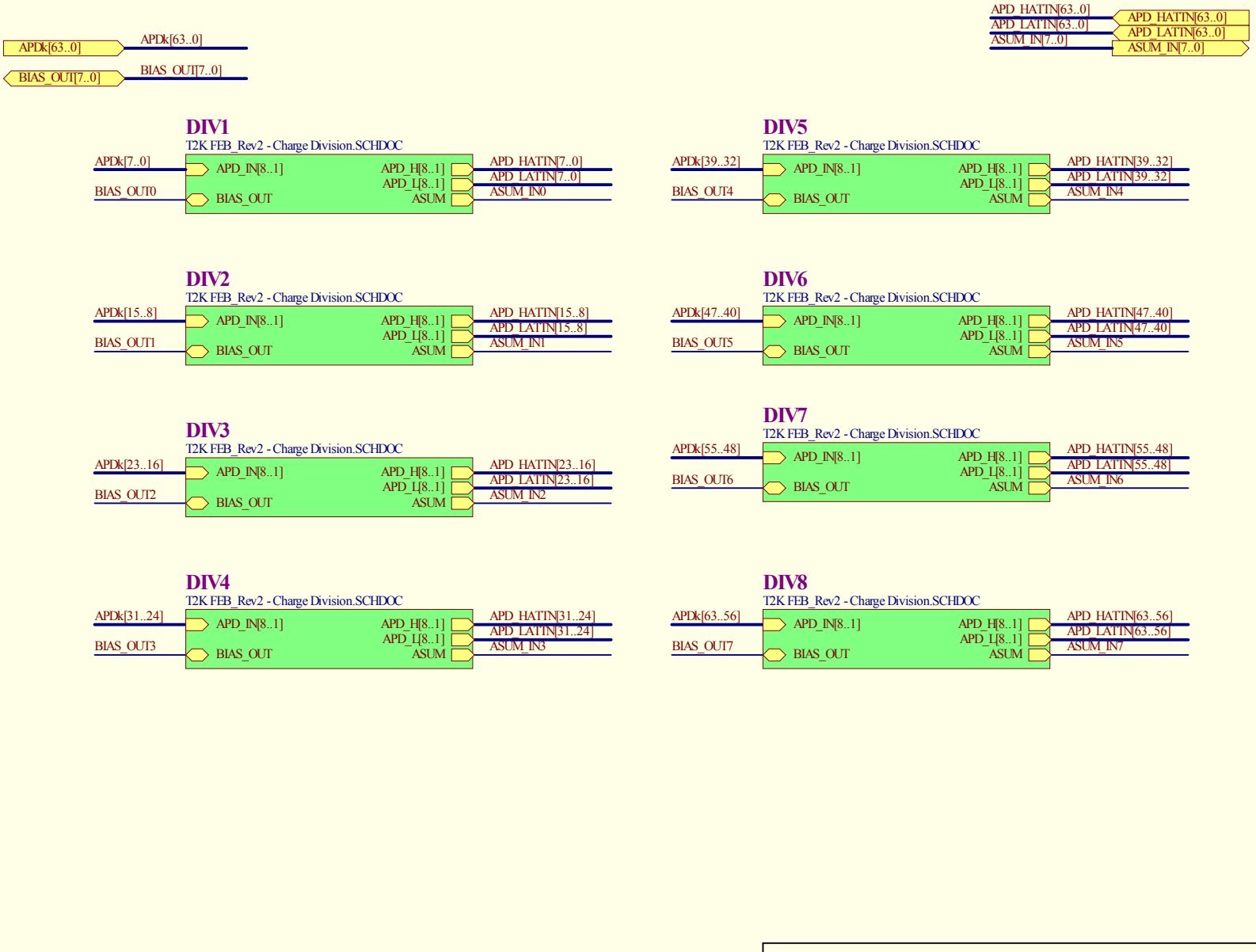
PAD1 PEM SMTSO-M3-3ET
PAD2 PEM SMTSO-M3-3ET
PAD3 PEM SMTSO-M3-3ET
PAD4 PEM SMTSO-M3-3ET
PAD5 PEM SMTSO-M3-3ET
PAD6 PEM SMTSO-M3-3ET
PAD7 PEM SMTSO-M3-3ET

T2K FEB - Top Level

TRIUMF LOGO

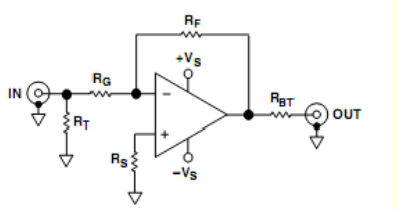
Revision	Drawing #: 1		
2	Sheet #: 1 of 16	Size: B	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Top Level.SCHDOC 5:10:18 PM

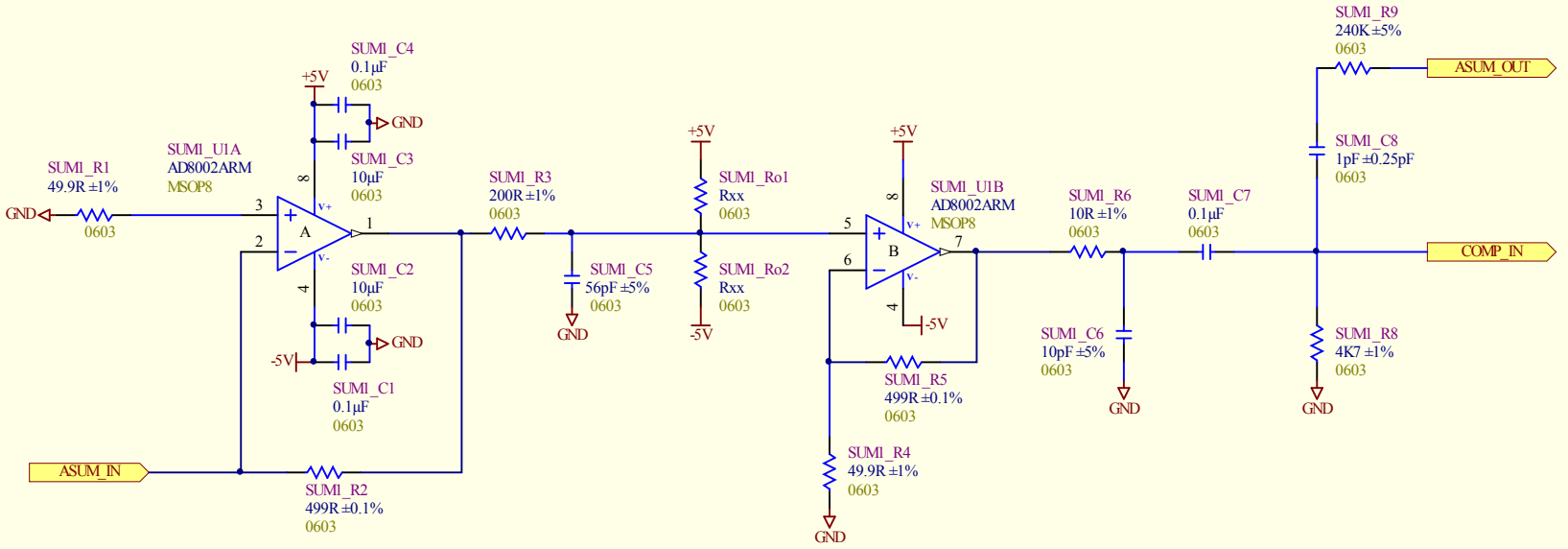

APDk[63..0]
APDk[63..0]
BIAS_OUT[7..0]
BIAS_OUT[7..0]
APD_HATIN[63..0]
APD_LATIN[63..0]
ASUM_IN[7..0]
APD_HATIN[63..0]
APD_LATIN[63..0]
ASUM_IN[7..0]
DIV1
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[7..0]
BIAS_OUT0
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[7..0]
APD_LATIN[7..0]
ASUM_IN0
DIV2
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[15..8]
BIAS_OUT1
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[15..8]
APD_LATIN[15..8]
ASUM_IN1
DIV3
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[23..16]
BIAS_OUT2
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[23..16]
APD_LATIN[23..16]
ASUM_IN2
DIV4
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[31..24]
BIAS_OUT3
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[31..24]
APD_LATIN[31..24]
ASUM_IN3
DIV5
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[39..32]
BIAS_OUT4
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[39..32]
APD_LATIN[39..32]
ASUM_IN4
DIV6
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[47..40]
BIAS_OUT5
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[47..40]
APD_LATIN[47..40]
ASUM_IN5
DIV7
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[55..48]
BIAS_OUT6
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[55..48]
APD_LATIN[55..48]
ASUM_IN6
DIV8
T2K FEB_Rev2 - Charge Division.SCHDOC
APDk[63..56]
BIAS_OUT7
APD_IN[8..1]
BIAS_OUT
APD_H[8..1]
APD_L[8..1]
ASUM
APD_HATIN[63..56]
APD_LATIN[63..56]
ASUM_IN7
T2K FEB64 - APD Inputs
Revision
2
Drawing #: 10
Sheet #: 10 of 16
Size: A
Drawn by: D.Bishop
Date: 10/12/2008
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - APD Inputs.SchDoc
5:10:18 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration

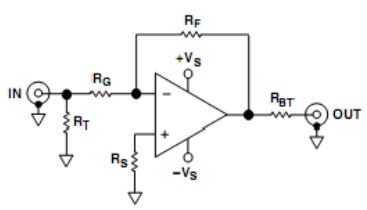


T2K FEB64 - Charge SUM Amplifier

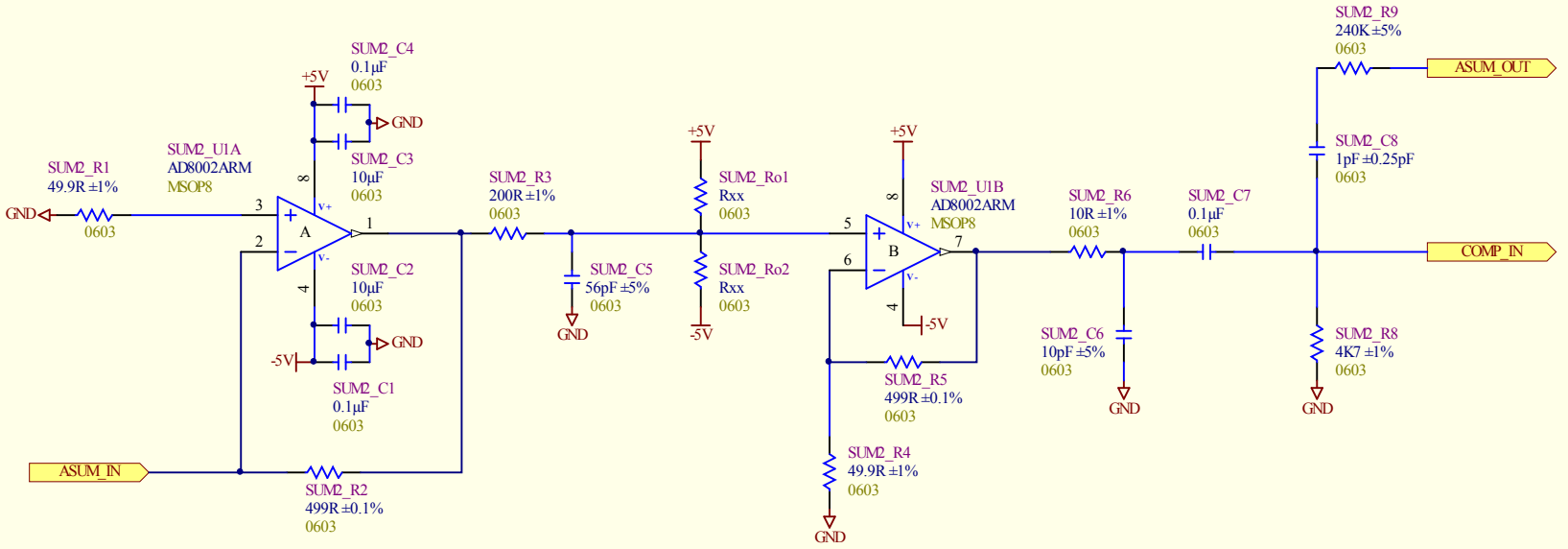
Revision	Drawing #: 11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:18 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration

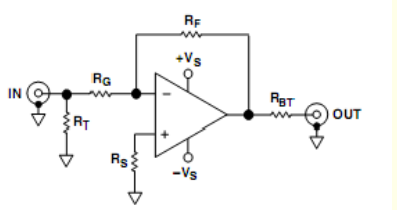


T2K FEB64 - Charge SUM Amplifier

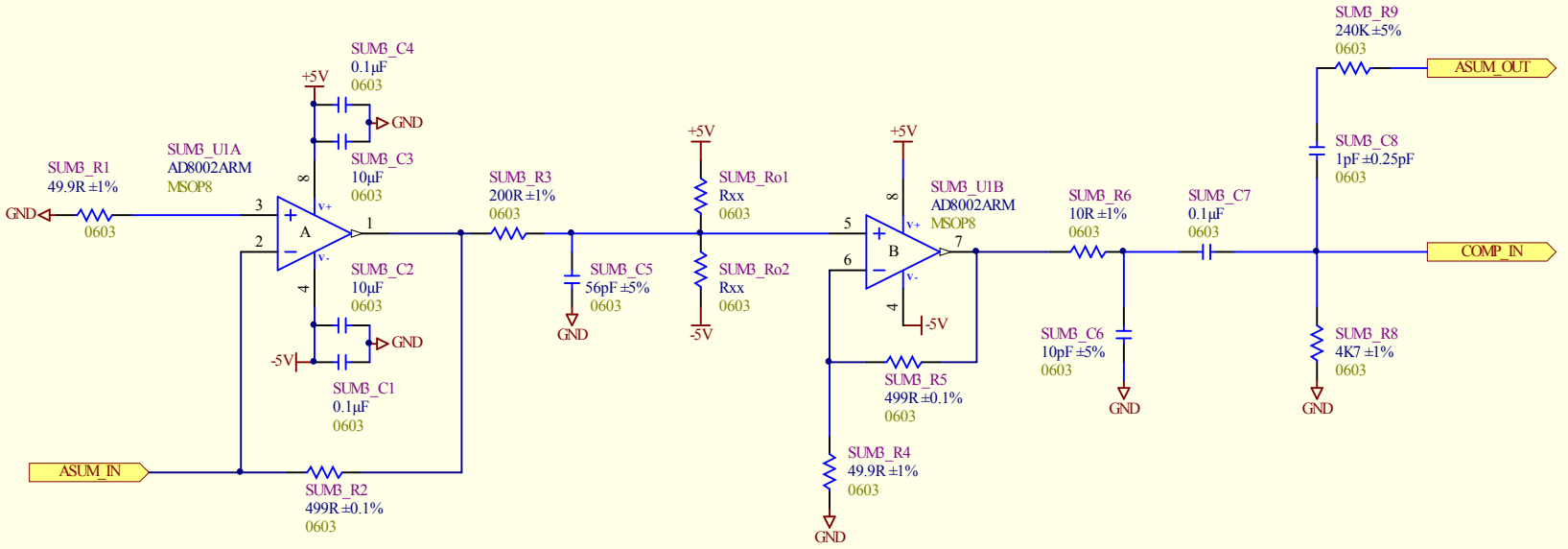
Revision	Drawing #: 11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:19 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration

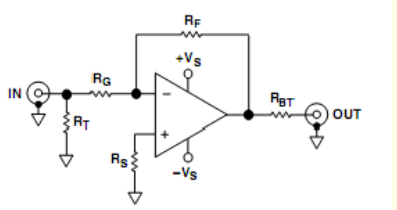


T2K FEB64 - Charge SUM Amplifier

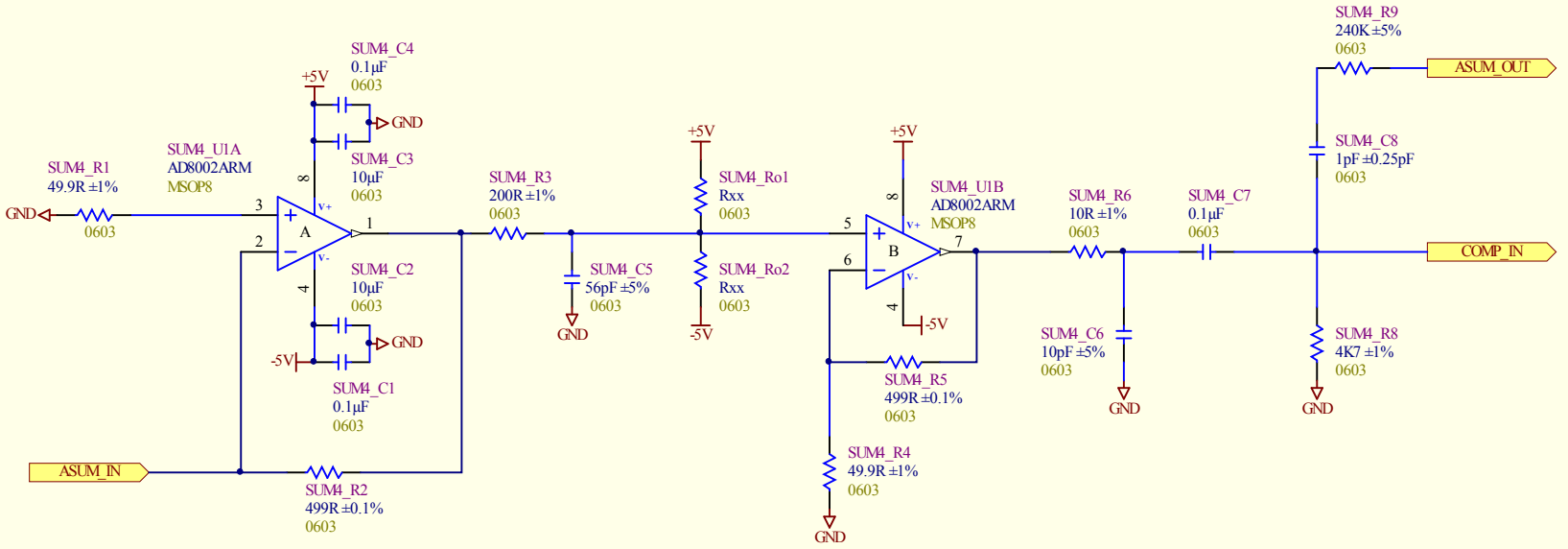
Revision 2	Drawing #: 11		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:19 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration

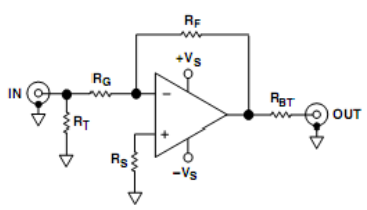


T2K FEB64 - Charge SUM Amplifier

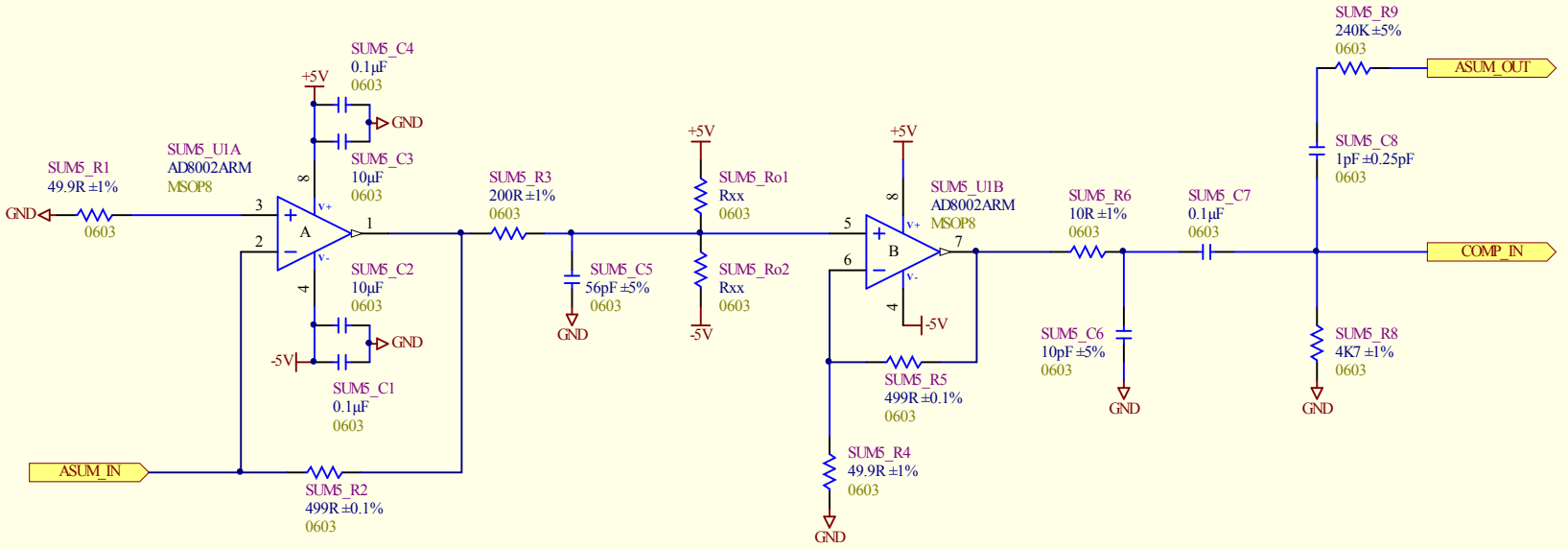
Revision	Drawing #: 11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:19 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration

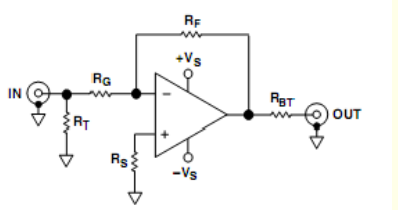


T2K FEB64 - Charge SUM Amplifier

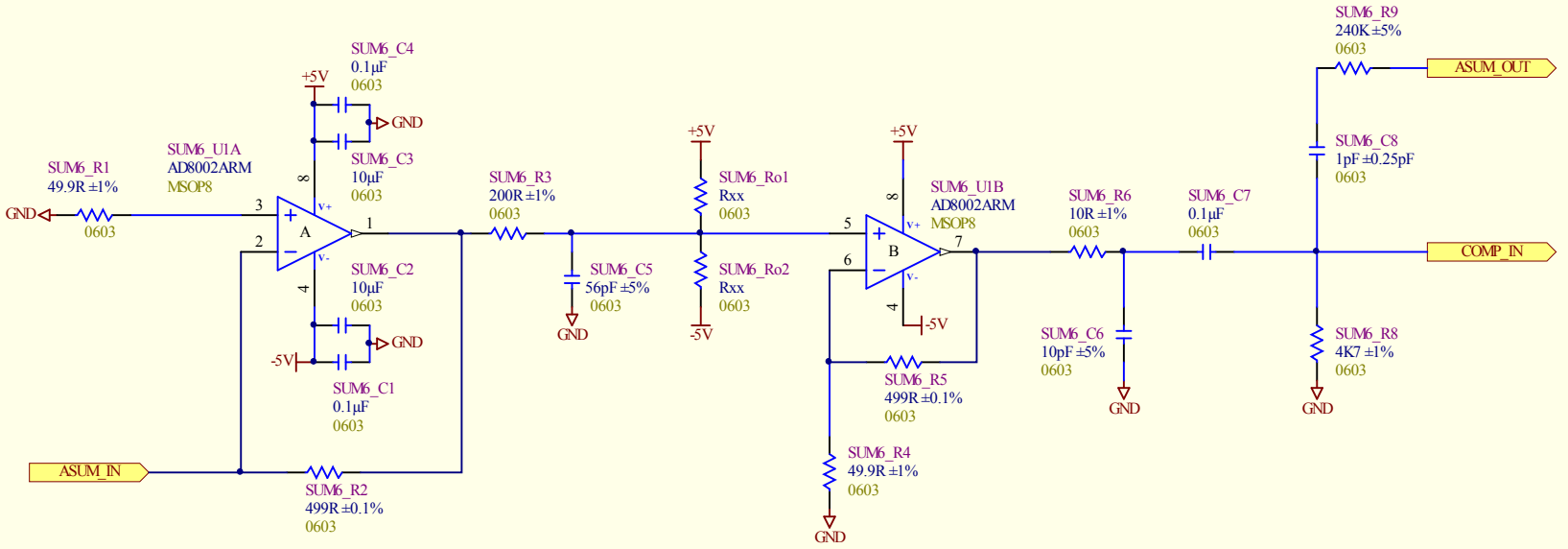
Revision 2	Drawing #: 11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:19 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration

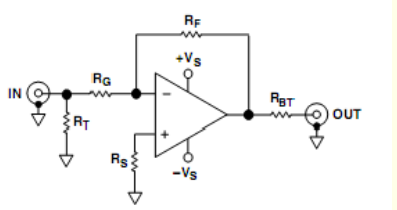


T2K FEB64 - Charge SUM Amplifier

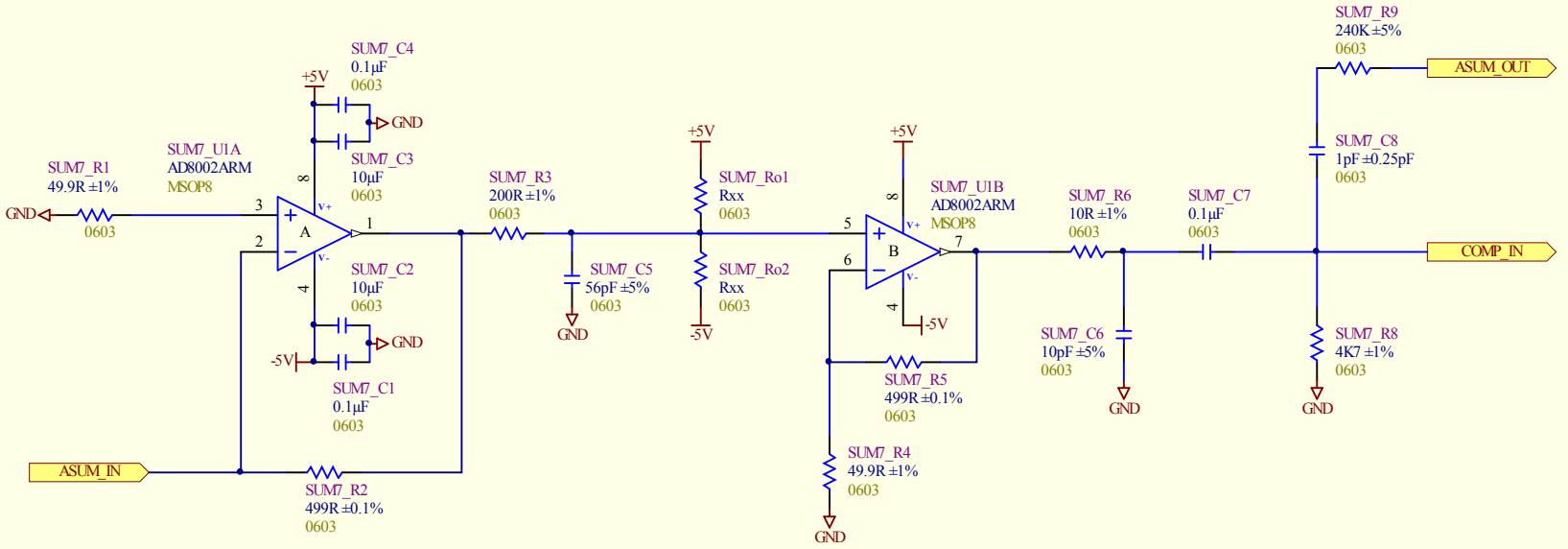
Revision 2	Drawing #: 11		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:19 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration

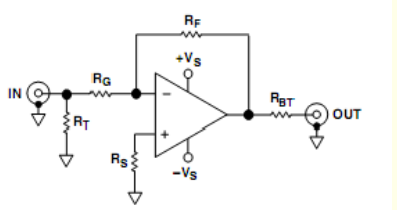


T2K FEB64 - Charge SUM Amplifier

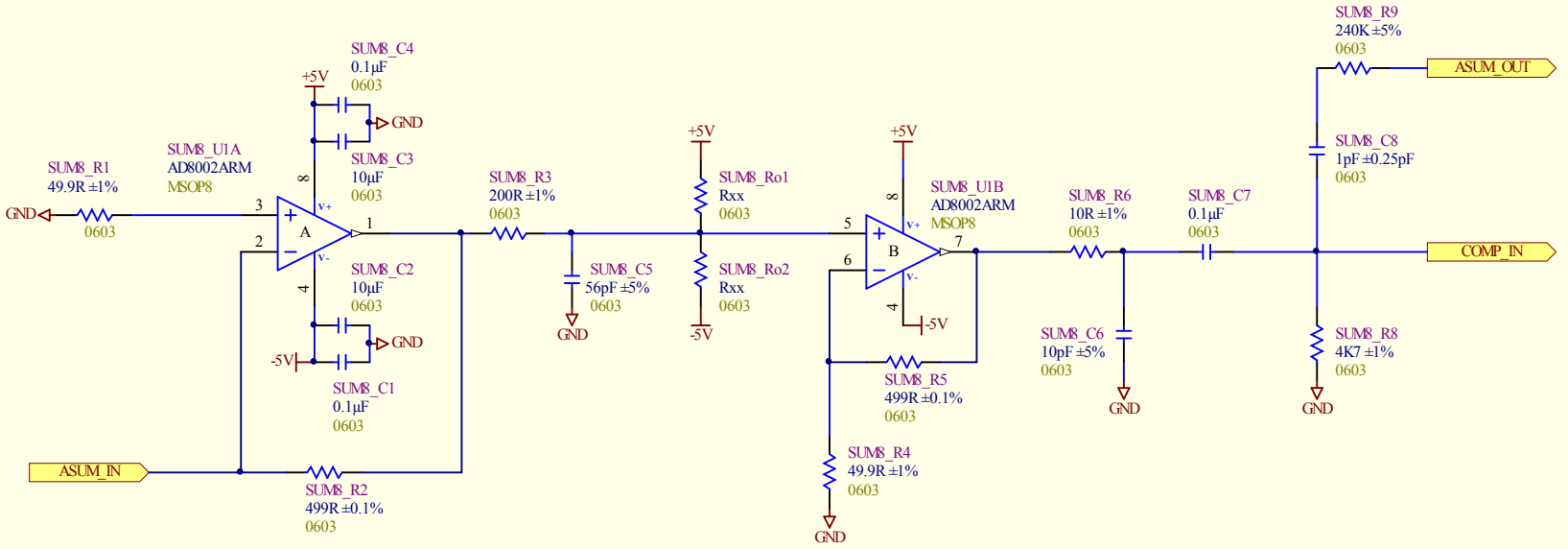
Revision 2	Drawing #: 11		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:19 PM

Component	AD8002ARM (µSOIC) Gain						
	–10	–2	–1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



Inverting Configuration



T2K FEB64 - Charge SUM Amplifier

Revision	Drawing #: 11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Analog SUM.SCHDOC			5:10:19 PM

SCA1_U1A

AFTER ASIC

InCh36	1	In_CH36
InCh35	2	In_CH35
InCh34	3	In_CH34
InCh33	4	In_CH33
InCh32	5	In_CH32
InCh31	6	In_CH31
InCh30	7	In_CH30
InCh29	8	In_CH29
InCh28	9	In_CH28
InCh27	10	In_CH27
InCh26	11	In_CH26
InCh25	12	In_CH25
InCh24	13	In_CH24
InCh23	14	In_CH23
InCh22	15	In_CH22
InCh21	16	In_CH21
InCh20	17	In_CH20
InCh19	18	In_CH19
InCh18	19	In_CH18
InCh17	20	In_CH17
InCh16	21	In_CH16
InCh15	22	In_CH15
InCh14	23	In_CH14
InCh13	24	In_CH13
InCh12	25	In_CH12
InCh11	26	In_CH11
InCh10	27	In_CH10
InCh09	28	In_CH9
InCh08	29	In_CH8
InCh07	30	In_CH7
InCh06	31	In_CH6
InCh05	32	In_CH5
InCh04	33	In_CH4
InCh03	34	In_CH3
InCh02	35	In_CH2
InCh01	36	In_CH1
3.3V (Ch1-36) Vdd_csag	37	AN_3.3V
(CH1 - 36) GND	38	GND
(Analog) In_cal	39	In_Cal
(Analog) In_testfonc	40	TestPulse

SCA1_U1B

AFTER ASIC

GND	41	GND
(3.3V) Vdd_crg	42	AN_3.3V
GND	43	GND
GND	44	
(3.3V) Vdd_skg	45	AN_3.3V
(Analog) Out_debug	46	Out_Debug
(3.3V) Vdd_g2g	47	AN_3.3V
GND	48	GND
GND	49	
(3.3V) Vdd	50	AN_3.3V
(CMOS) - Sc_din	51	Sc_din
(CMOS) - Sc_en	52	Sc_en
(CMOS) - Sc_ck	53	Sc_ck
(CMOS) - Sc_dout	54	Sc_dout
(3.3V) Vdd_prob	55	AN_3.3V
(CMOS) - read	56	read
(LVDS) - rckm	57	rck_N
(LVDS) - rckp	58	rck_P
(LVDS) - wckm	59	wck_N
(LVDS) - wckp	60	wck_P
(CMOS) - write	61	write
(3.3V) Vdd	62	AN_3.3V
GND	63	
GND	64	GND
(3.3V) Vdd	65	
(3.3V) Vdd	66	AN_3.3V
GND	67	GND
(VddADC/2) vocm	68	1.65V
(Curr 2ma) Vgg1	69	Vgg1
(Curr 1ma) Vgg7	70	Vgg7
(1.45V) vicm	71	Vicm
(3.3V) Vdd_out	72	AN_3.3V
(Analog) vop	73	Vo_P
(Analog) vom	74	Vo_N
GND	75	
GND	76	
(3.3V) Vdd_g2d	77	GND
GND	78	AN_3.3V
(3.3V) Vdd_skd	79	GND
GND	80	AN_3.3V
		GND

SCA1_U1C

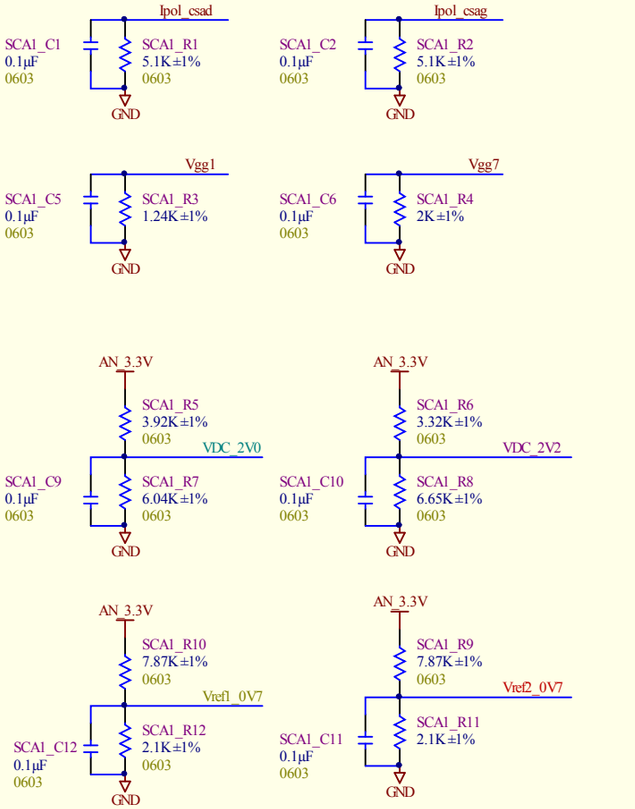
AFTER ASIC

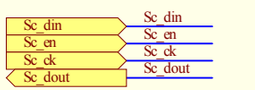
GND	81	GND
(3.3V) Vdd_crd	82	AN_3.3V
GND	83	GND
(3.3V) Vdd_csad	84	AN_3.3V
InCh72	85	In_CH72
InCh71	86	In_CH71
InCh70	87	In_CH70
InCh69	88	In_CH69
InCh68	89	In_CH68
InCh67	90	In_CH67
InCh66	91	In_CH66
InCh65	92	In_CH65
InCh64	93	In_CH64
InCh63	94	In_CH63
InCh62	95	In_CH62
InCh61	96	In_CH61
InCh60	97	In_CH60
InCh59	98	In_CH59
InCh58	99	In_CH58
InCh57	100	In_CH57
InCh56	101	In_CH56
InCh55	102	In_CH55
InCh54	103	In_CH54
InCh53	104	In_CH53
InCh52	105	In_CH52
InCh51	106	In_CH51
InCh50	107	In_CH50
InCh49	108	In_CH49
InCh48	109	In_CH48
InCh47	110	In_CH47
InCh46	111	In_CH46
InCh45	112	In_CH45
InCh44	113	In_CH44
InCh43	114	In_CH43
InCh42	115	In_CH42
InCh41	116	In_CH41
InCh40	117	In_CH40
InCh39	118	In_CH39
InCh38	119	In_CH38
InCh37	120	In_CH37

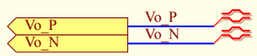
SCA1_U1D

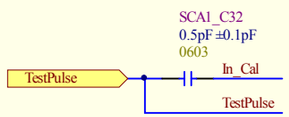
AFTER ASIC

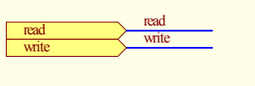
GND	121	
GND	122	GND
(3.3V) Vdd_proind	123	
(3.3V) Vdd_csad	124	AN_3.3V
GND	125	GND
(Current) Ipol_csad	126	Ipol_csad
(3.3V) Vdd_crd	127	AN_3.3V
GND	128	GND
(3.3V) Vdd_skd	129	AN_3.3V
GND	130	GND
(3.3V) Vdd_g2d	131	AN_3.3V
GND	132	GND
(2V) Vdc_csad	133	VDC_2V0
(2.2V) Vdc_cd	134	VDC_2V2
(0.7V) Vdc_g2d	135	Vref2_0V7
(3.3V) Vdd	136	AN_3.3V
GND	137	GND
(0.7V) vref_scad	138	Vref1_0V7
(Analog I) vb_ra	139	Vb_ra
(3.3V) Vdd_proh	140	AN_3.3V
GND	141	GND
(0.7V) vref_scag	142	Vref1_0V7
(Analog I) vbf	143	Vbf
(3.3V) Vdd	144	AN_3.3V
GND	145	GND
(0.7V) Vdc_g2g	146	Vref2_0V7
(2.2V) Vdc_cg	147	VDC_2V2
(2V) Vdc_csag	148	VDC_2V0
GND	149	GND
(3.3V) Vdd_g2g	150	AN_3.3V
GND	151	GND
(3.3V) Vdd_skg	152	AN_3.3V
GND	153	GND
(3.3V) Vdd_crg	154	AN_3.3V
(Current) Ipol_csag	155	Ipol_csag
GND	156	GND
(3.3V) Vdd_csag	157	
(3.3V) Vdd_proing	158	AN_3.3V
GND	159	
GND	160	GND

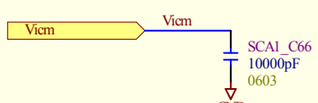


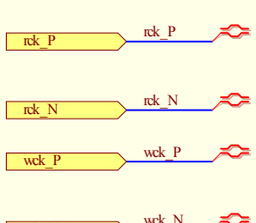


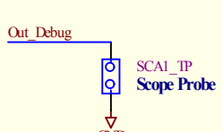






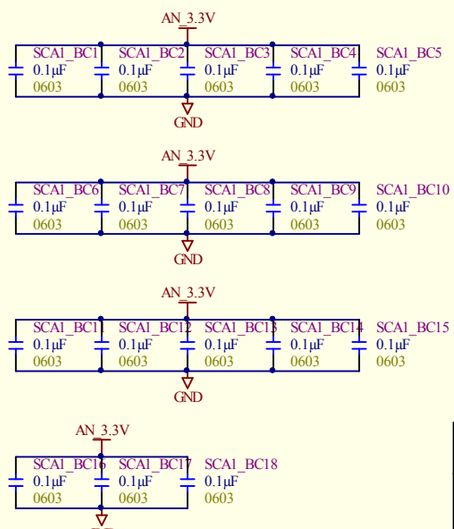


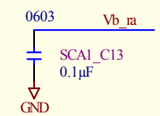


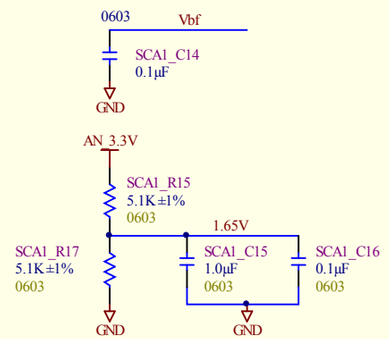


Pin 37	**Vdd_csag**	9.83	**CSA**
Pin 157	**Vdd_csag**	9.83	
Pin 84	**Vdd_csad**	9.83	
Pin 124	**Vdd_csad**	9.83	
Pin 42	**Vdd_crg**	3.9	CR Filter
Pin 154	**Vdd_crg**	3.9	
Pin 82	**Vdd_crd**	3.9	
Pin 127	**Vdd_crd**	3.9	
Pin 45	**Vdd_skg**	1.9	SK Filter
Pin 152	**Vdd_skg**	1.9	
Pin 79	**Vdd_skd**	1.9	
Pin 129	**Vdd_skd**	1.9	
Pin 47	**Vdd_g2g**	6.881	Gain-2
Pin 150	**Vdd_g2g**	6.881	
Pin 77	**Vdd_g2d**	6.881	
Pin 131	**Vdd_g2d**	6.881	
Pin 50	**Vdd**	3.676	
Pin 144	**Vdd**	3.676	
Pin 66	**Vdd**	6.62	
Pin 136	**Vdd**	6.62	
Pin 62	**Vdd**	0.343	
Pin 65	**Vdd**	0	
Pin 72	**Vdd_out**	16.03	
Pin 126	**Ipol_csad**	0.2	
Pin 155	**Ipol_csag**	0.2	
Pin 69	**Vgg1**	2	
Pin 70	**Vgg7**	1	

130.41 **260.818**



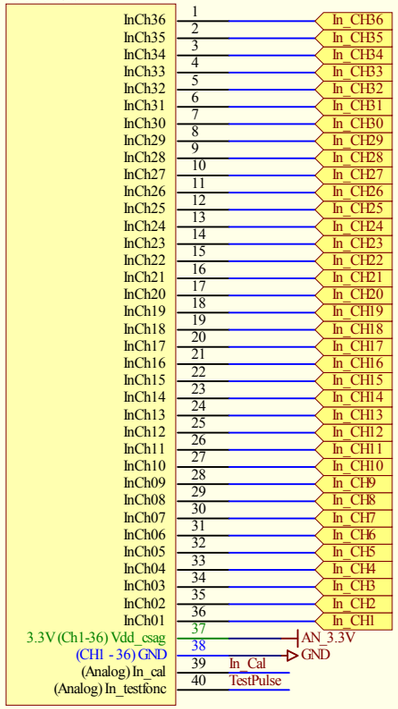




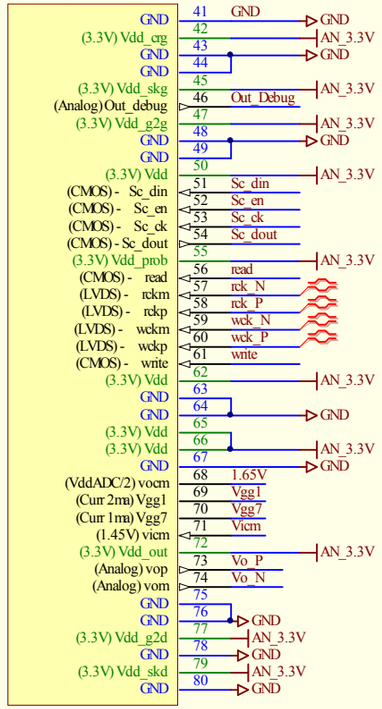
T2K FEB64 - AFTER ASIC

Revision 2	Drawing #: 12		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 12 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - AFTER ASIC.SCHDOC			5:10:19 PM

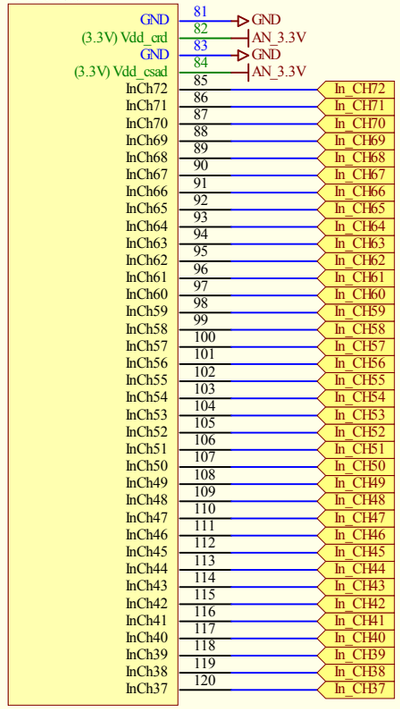
SCA2_U1A
AFTER ASIC



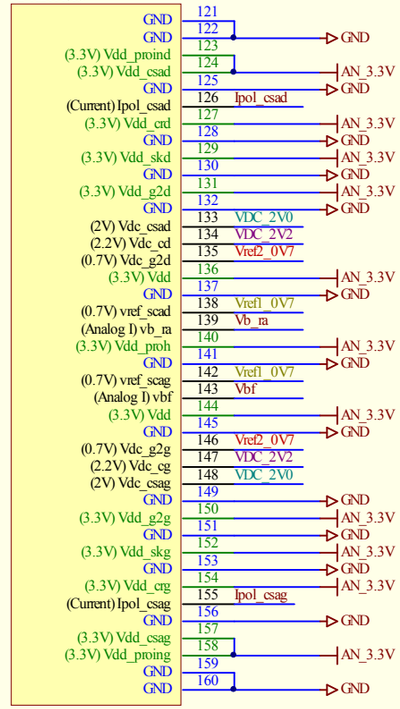
SCA2_U1B
AFTER ASIC

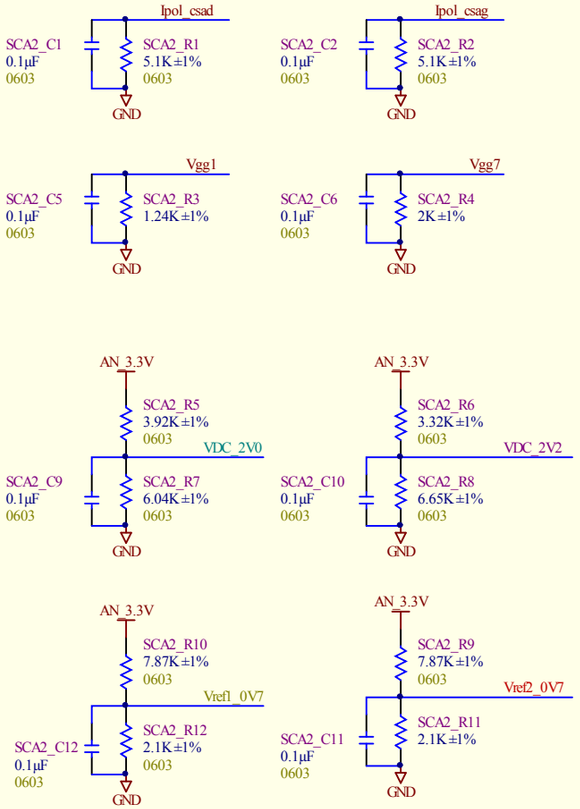


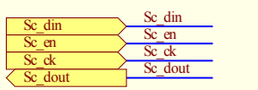
SCA2_U1C
AFTER ASIC

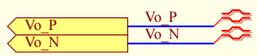


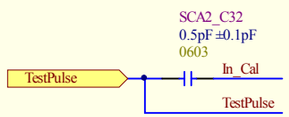
SCA2_U1D
AFTER ASIC

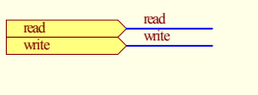


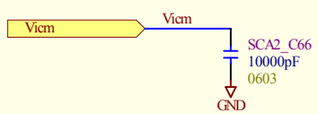


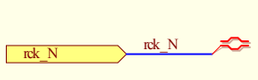


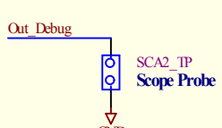






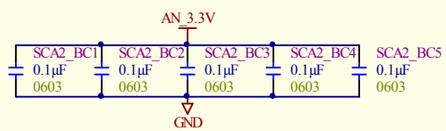


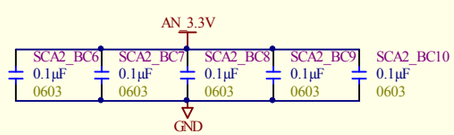


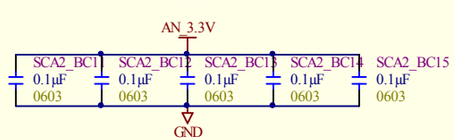


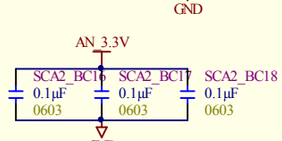
Pin 37	**Vdd_csag**	9.83	**CSA**
Pin 157	**Vdd_csag**	9.83	
Pin 84	**Vdd_csad**	9.83	
Pin 124	**Vdd_csad**	9.83	
Pin 42	**Vdd_crg**	3.9	CR Filter
Pin 154	**Vdd_crg**	3.9	
Pin 82	**Vdd_crd**	3.9	
Pin 127	**Vdd_crd**	3.9	
Pin 45	**Vdd_skg**	1.9	SK Filter
Pin 152	**Vdd_skg**	1.9	
Pin 79	**Vdd_skd**	1.9	
Pin 129	**Vdd_skd**	1.9	
Pin 47	**Vdd_g2g**	6.881	Gain-2
Pin 150	**Vdd_g2g**	6.881	
Pin 77	**Vdd_g2d**	6.881	
Pin 131	**Vdd_g2d**	6.881	
Pin 50	**Vdd**	3.676	
Pin 144	**Vdd**	3.676	
Pin 66	**Vdd**	6.62	
Pin 136	**Vdd**	6.62	
Pin 62	**Vdd**	0.343	
Pin 65	**Vdd**	0	
Pin 72	**Vdd_out**	16.03	
Pin 126	**Ipol_csad**	0.2	
Pin 155	**Ipol_csag**	0.2	
Pin 69	**Vgg1**	2	
Pin 70	**Vgg7**	1	

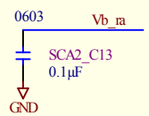
130.41 **260.818**

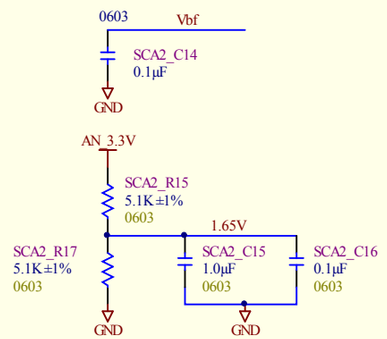






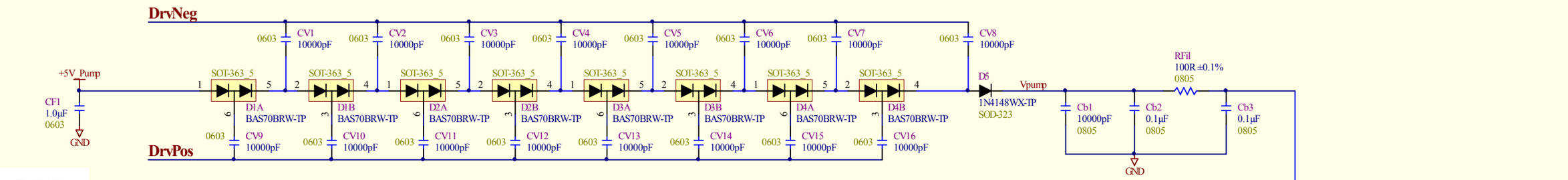


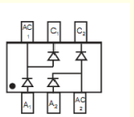


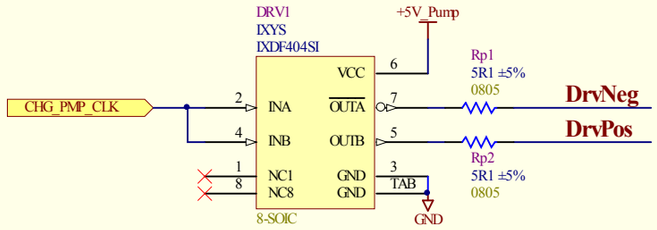


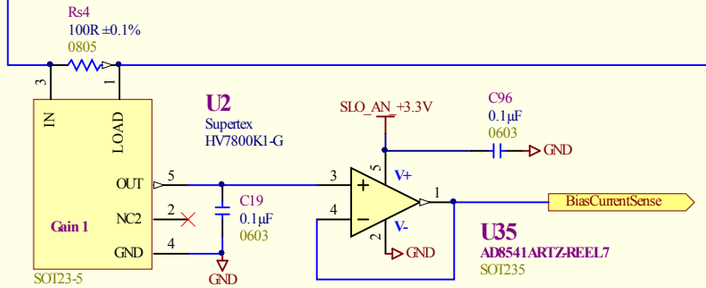
T2K FEB64 - AFTER ASIC

Revision **2**	Drawing #: 12		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 12 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - AFTER ASIC.SCHDOC			5:10:19 PM









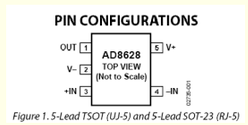
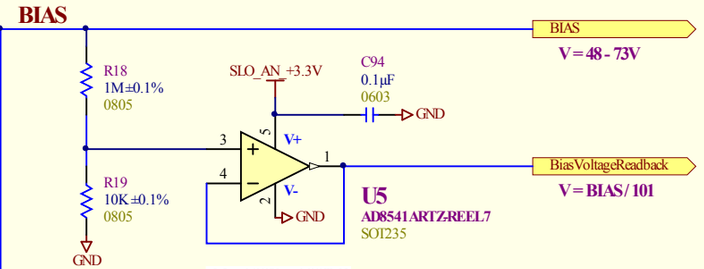
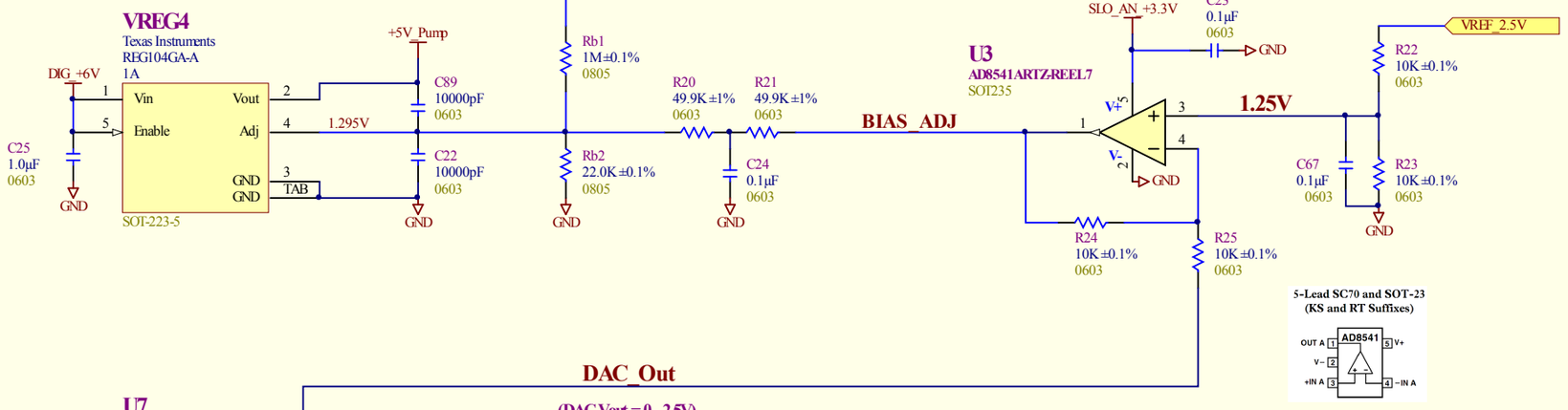
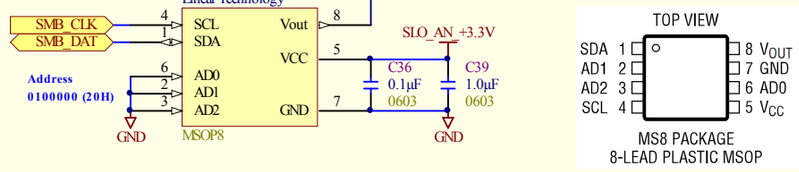


Figure 1. 5-Lead TSOT (UJ-5) and 5-Lead SOT-23 (RJ-5)

Alternate OP Amps
LTC2054CS5#TRMPBF
AD8628AUJZ-REEL7







HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

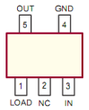
-G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



5-Lead SOT-23
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} [1]	-0.5V to +450V
V_{OUT} [1]	-0.5V to +10V
V_{SENSE} [2]	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

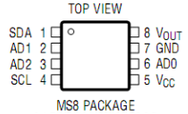
Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
— = "Green" Packaging

5-Lead SOT-23

PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER	
LTC1669CMS8	LTC1669-8CMS8
LTC1669IMS8	LTC1669-8IMS8
MS8 PART MARKING	
LTAHV	LTAHT
LTAHX	LTAHU

T2K FEB64: BIAS / Total Bias Current Sense

Revision 2	Drawing #: 13		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 13 of 16	Size: B	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - 80 Volt Charge Pump.SCHDOC			5:10:20 PM

U14

Analog Devices
AD9229BCPZ-50

ADC_VINA_P
ADC_VINA_N
ADC_VINB_P
ADC_VINB_N
ADC_VINC_P
ADC_VINC_N
ADC_VIND_P
ADC_VIND_N
AD9229_VREF
ADC_CLK
ADC_DTP
ADC_PDWN

VIN+ A (10) / VIN- A (11)
VIN+ B (14) / VIN- B (13)
VIN+ C (23) / VIN- C (24)
VIN+ D (27) / VIN- D (26)
VREF (18)
SENSE (17)
REFT (20)
REFB (19)
AGND (6, 9, 12, 15, 22, 25, 28, 31, 33, 49)
CASE_AGND
DRGND (1, 36)

D+A (44) / D- A (43)
D+B (42) / D- B (41)
D+C (40) / D- C (39)
D+D (38) / D- D (37)
FCO+ (46) / FCO- (45)
DCO+ (48) / DCO- (47)
CLK (30)
LVDS_BIAS (34)
DTP (4)
PWDN (7)
AVDD (32, 29, 21, 16, 8, 5)
NC3 (3)
DRVDD (35, 2)

LVDS_ADC_DATA0_P
LVDS_ADC_DATA0_N
LVDS_ADC_DATA1_P
LVDS_ADC_DATA1_N
LVDS_ADC_DATA2_P
LVDS_ADC_DATA2_N
LVDS_ADC_DATA3_P
LVDS_ADC_DATA3_N
LVDS_ADC_FCO_P
LVDS_ADC_FCO_N
LVDS_ADC_DCO_P
LVDS_ADC_DCO_N

C47 10µF 0603
C48 0.1µF 0603
C49 0.1µF 0603
C50 0.1µF 0603
C51 0.1µF 0603
C52 10µF 0603
C53 0.1µF 0603
C54 0.1µF 0603
C55 0.1µF 0603
C57 0.1µF 0603
C58 0.1µF 0603
C59 0.1µF 0603
C60 0.1µF 0603
C90 0.1µF 0603
R59 4K7 ±1% 0603
R46 4K7 ±1% 0603

GND
+3.3V
AN_3.3V

48-LFCSP

AD9229

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

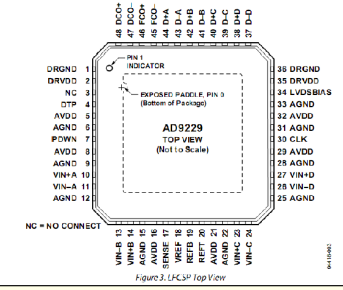


Figure 3. LFCSP Top View

C41 0.1µF 0603

U13

Texas Instruments
SN65LVDS2DBVR

LVDS_ADC_CLK_P
LVDS_ADC_CLK_N
ADC_CLK
R17 100R 1% 0603
Vcc
R2
Gnd
SOT23-5

T2K FEB64 - 65M SPS ADC			
Revision 2	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - 50MSPS ADC.SCHDOC			5:10:20 PM

APD_DAC[63..0] → APD_DAC[63..0]

APD_DAC_CSn[7..0] → APD_DAC_CSn[7..0]

APD_DAC_SCK
APD_DAC_DIN
DAC_ResetN

Pin Compatible Versions

LTC2600: 16-Bits
LTC2610: 14-Bits
LTC2620: 12-Bits
LTC1660: 10-Bits
LTC1665: 8-Bits

U22
Linear Technology
LTC1665CGN#PBF
SSOP16

APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn0, DAC_ResetN

RP3 0603 x 4: APD_DAC7, APD_DAC6, APD_DAC5, APD_DAC4
RP4 0603 x 4: APD_DAC3, APD_DAC2, APD_DAC1, APD_DAC0

REF 6 — VCC 16 (+5V, C169 0.1µF 0603) — GND 1 (GND)

U24
Linear Technology
LTC1665CGN#PBF
SSOP16

APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn1, DAC_ResetN

RP7 0603 x 4: APD_DAC15, APD_DAC14, APD_DAC13, APD_DAC12
RP8 0603 x 4: APD_DAC11, APD_DAC10, APD_DAC9, APD_DAC8

REF 6 — VCC 16 (+5V, C187 0.1µF 0603) — GND 1 (GND)

U26
Linear Technology
LTC1665CGN#PBF
SSOP16

APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn2, DAC_ResetN

RP11 0603 x 4: APD_DAC23, APD_DAC22, APD_DAC21, APD_DAC20
RP12 0603 x 4: APD_DAC19, APD_DAC18, APD_DAC17, APD_DAC16

REF 6 — VCC 16 (+5V, C205 0.1µF 0603) — GND 1 (GND)

U28
Linear Technology
LTC1665CGN#PBF
SSOP16

APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn3, DAC_ResetN

RP15 0603 x 4: APD_DAC31, APD_DAC30, APD_DAC29, APD_DAC28
RP16 0603 x 4: APD_DAC27, APD_DAC26, APD_DAC25, APD_DAC24

REF 6 — VCC 16 (+5V, C207 0.1µF 0603) — GND 1 (GND)

U23
Linear Technology
LTC1665CGN#PBF
SSOP16

APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn4, DAC_ResetN

RP5 0603 x 4: APD_DAC39, APD_DAC38, APD_DAC37, APD_DAC36
RP6 0603 x 4: APD_DAC35, APD_DAC34, APD_DAC33, APD_DAC32

REF 6 — VCC 16 (+5V, C170 0.1µF 0603) — GND 1 (GND)

U25
Linear Technology
LTC1665CGN#PBF
SSOP16

APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn5, DAC_ResetN

RP9 0603 x 4: APD_DAC47, APD_DAC46, APD_DAC45, APD_DAC44
RP10 0603 x 4: APD_DAC43, APD_DAC42, APD_DAC41, APD_DAC40

REF 6 — VCC 16 (+5V, C188 0.1µF 0603) — GND 1 (GND)

U27
Linear Technology
LTC1665CGN#PBF
SSOP16

APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn6, DAC_ResetN

RP13 0603 x 4: APD_DAC55, APD_DAC54, APD_DAC53, APD_DAC52
RP14 0603 x 4: APD_DAC51, APD_DAC50, APD_DAC49, APD_DAC48

REF 6 — VCC 16 (+5V, C206 0.1µF 0603) — GND 1 (GND)

U29
Linear Technology
LTC1665CGN#PBF
SSOP16

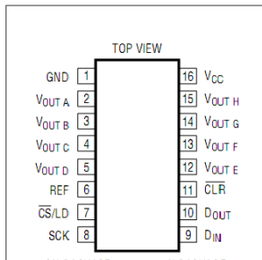
APD_DAC_SCK, APD_DAC_DIN, APD_DAC_CSn7, DAC_ResetN

RP17 0603 x 4: APD_DAC63, APD_DAC62, APD_DAC61, APD_DAC60
RP18 0603 x 4: APD_DAC59, APD_DAC58, APD_DAC57, APD_DAC56

REF 6 — VCC 16 (+5V, C208 0.1µF 0603) — GND 1 (GND)

CP1 0.1µF 0612: APD_DAC0, APD_DAC1, APD_DAC2, APD_DAC3 → GND
CP2 0.1µF 0612: APD_DAC4, APD_DAC5, APD_DAC6, APD_DAC7 → GND
CP3 0.1µF 0612: APD_DAC8, APD_DAC9, APD_DAC10, APD_DAC11 → GND
CP4 0.1µF 0612: APD_DAC12, APD_DAC13, APD_DAC14, APD_DAC15 → GND
CP5 0.1µF 0612: APD_DAC16, APD_DAC17, APD_DAC18, APD_DAC19 → GND
CP6 0.1µF 0612: APD_DAC20, APD_DAC21, APD_DAC22, APD_DAC23 → GND
CP7 0.1µF 0612: APD_DAC24, APD_DAC25, APD_DAC26, APD_DAC27 → GND
CP8 0.1µF 0612: APD_DAC28, APD_DAC29, APD_DAC30, APD_DAC31 → GND
CP9 0.1µF 0612: APD_DAC32, APD_DAC33, APD_DAC34, APD_DAC35 → GND
CP10 0.1µF 0612: APD_DAC36, APD_DAC37, APD_DAC38, APD_DAC39 → GND
CP11 0.1µF 0612: APD_DAC40, APD_DAC41, APD_DAC42, APD_DAC43 → GND
CP12 0.1µF 0612: APD_DAC44, APD_DAC45, APD_DAC46, APD_DAC47 → GND
CP13 0.1µF 0612: APD_DAC48, APD_DAC49, APD_DAC50, APD_DAC51 → GND
CP14 0.1µF 0612: APD_DAC52, APD_DAC53, APD_DAC54, APD_DAC55 → GND
CP15 0.1µF 0612: APD_DAC56, APD_DAC57, APD_DAC58, APD_DAC59 → GND
CP16 0.1µF 0612: APD_DAC60, APD_DAC61, APD_DAC62, APD_DAC63 → GND

PACKAGE/ORDER INFORMATION



GN PACKAGE 16-LEAD PLASTIC SSOP
N PACKAGE 16-LEAD PDIP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W (GN)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)

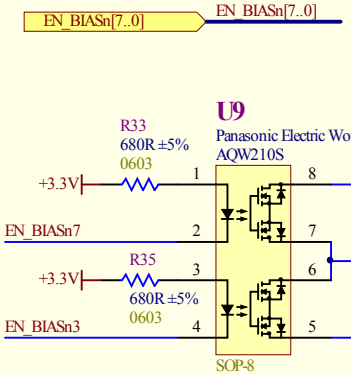
ORDER PART NUMBER
LTC1665CGN
LTC1665CN
LTC1665IGN
LTC1665IN
LTC1660CGN
LTC1660CN
LTC1660IGN
LTC1660IN

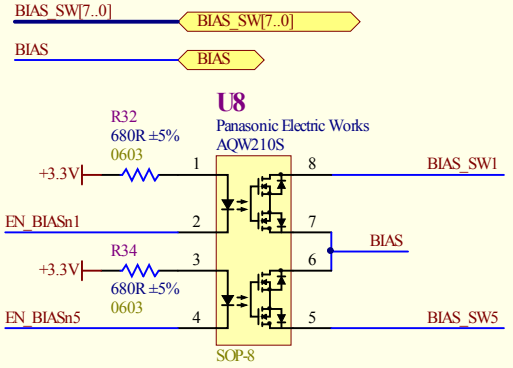
GN PART MARKING	
1665	1660
1665I	1660I

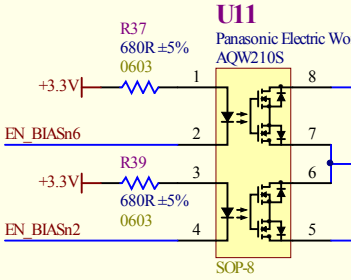
T2K FEB64 - 64 Channel Bias Control

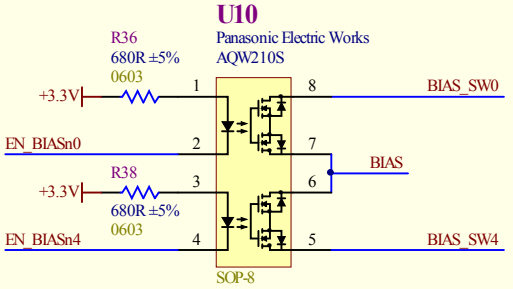
Revision	Drawing #: 15		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 15 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - 64 Channel Bias Control.SCHDOC 10:20 PM





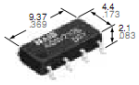




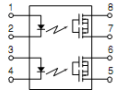
Panasonic
ideas for life

Super miniature design, SOP (2 Form A) 8-pin type. Controls load voltage 350V, 400V.

GU PhotoMOS (AQW21○S)

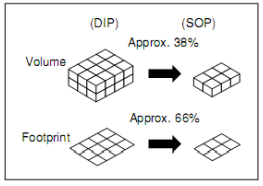


mm inch



FEATURES

1. 2 channels in super miniature design
The device comes in a super-miniature SO package measuring (W) 4.4 × (L) 9.37 × (H) 2.1 mm (W) .173× (L) .369× (H) .083 inch —approx. 38% of the volume and 66% of the footprint size of DIP type PhotoMOS Relays.



2. Tape and reel
The device comes standard in a tape and reel (1,000 pcs./reel) to facilitate automatic insertion machines.

3. Controls low-level analog signals
PhotoMOS relays feature extremely low closed-circuit offset voltage to enable control of low-level analog signals without distortion.

4. Low-level off state leakage current
In contrast to the SSR with an off state leakage current of several milliamperes, the PhotoMOS relay features a very small off state leakage current of typ. 100 pA even with the rated load voltage of 400 V (AQW214S)

TYPICAL APPLICATIONS

- Telephones
- Measuring instruments
- Computer
- Industrial robots
- High-speed inspection machines.

T2K FEB64 - 8 Channel Mosfet Switch

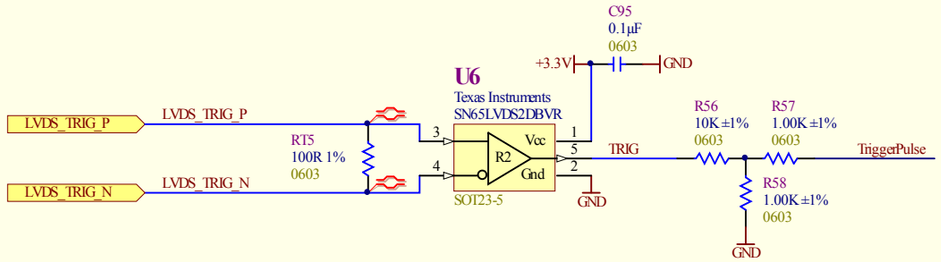
Revision	Drawing #: 16		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 16 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

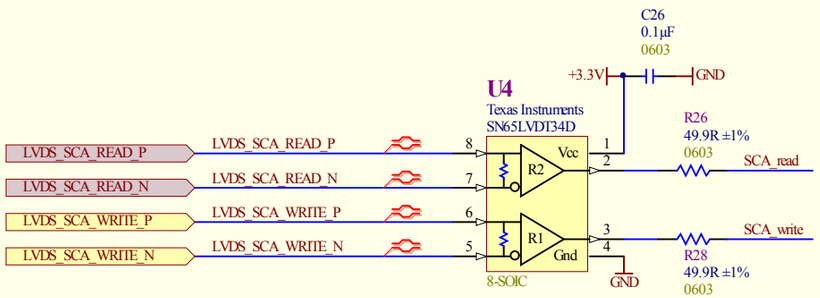
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - 8 Channel MOSFET Switch.SCHDOC 3:20 PM

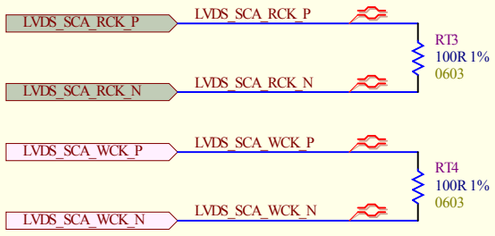
ASUM_OUT[7..0]

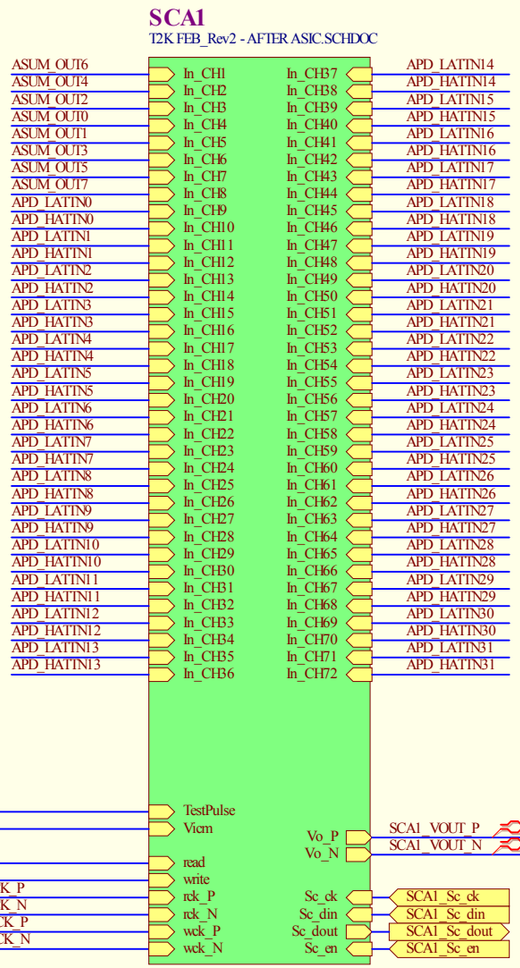
APD_HATIN[63..0]

APD_LATIN[63..0]

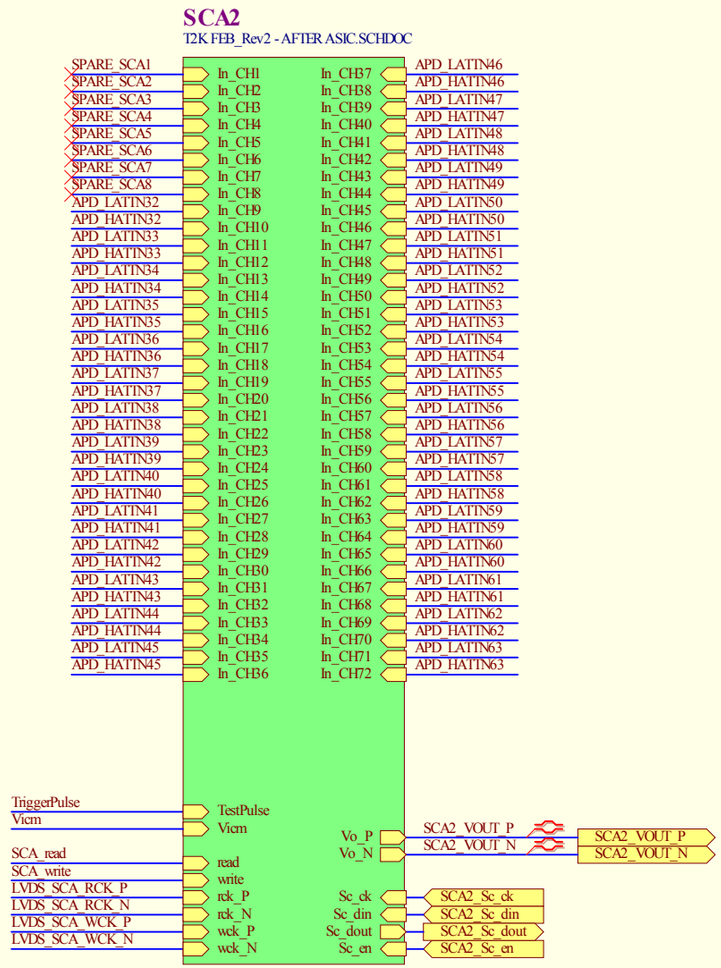




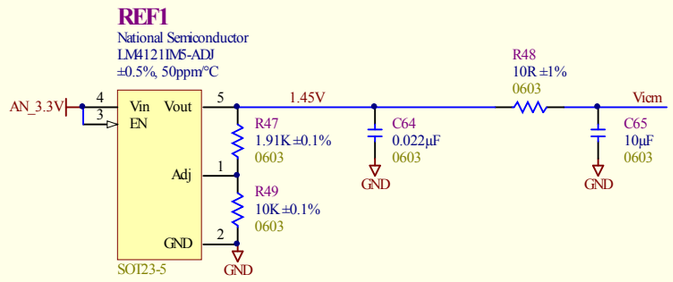




SCA - Icc approx 130ma



SCA - Icc approx 130ma



Vout = 1.216V(1+R47/R49)

Vout = 1.216V(1.191) = 1.448 Volts

Vicm= +60uA / -26uA

T2K FEB64: SCA Interface

Revision 2	Drawing #: 2		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 2 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - SCA Interface.SCHDOC			5:10:20 PM

VREG7

Texas Instruments
REG104GA-3.3
1A

+5V — C42 1.0µF 0603 — GND
Vin (1), Enable (5), Vout (2) → AN_3.3V, NR (4) → C43 10000pF 0603 → GND, GND, TAB (3) → GND
SOT-223-5

3.3V for 50MSPS ADC and SCA1,2

VREG5

LD2981CU33TR

C85 1.0µF 0805 — GND
Vin (3), GND (2), Vout (1) → SLO_AN +3.3V → C33 10µF 0805 → GND
SOT89

SLO +5V

VREG6

LD2981CU33TR

C93 1.0µF 0805 — GND
Vin (3), GND (2), Vout (1) → SLO_+3.3V → C35 10µF 0805 → GND
SOT89

VREG2

Texas Instruments
REG104GA-5
1A

C46 10µF 1206 — GND
C61 10µF 1206 — GND
AN +6V → Vin (1)
REG_Enable → Enable (5)
Vout (2) → +5V → C86 6.8µF 1206 → GND
NR/Adj (4) → C147 10000pF 0805
GND, GND, TAB (3) → GND
SOT-223-5

VREG1

REG104GA-3.3
1A

C44 10µF 1206 — GND
C45 10µF 1206 — GND
DIG +6V → Vin (1)
REG_Enable → Enable (5)
Vout (2) → +3.3V → C72 6.8µF 1206 → GND
NR/Adj (4) → C144 10000pF 0805
GND, GND, TAB (3) → GND
SOT-223-5

VREG3

LT1175CS8-5#PBF
500ma

C62 10µF 1206 — GND
C63 10µF 1206 — GND
AN -6V → VIN (1)
REG_Enable → SHDWN (6)
VIN (8), ILIM2 (2), ILIM4 (7), GND (5)
VOUT (3) → -5V → C71 6.8µF 1206 → GND
SENSE (4)
8-SOIC

U33

Rs2
Panasonic - ECG
0.050R ±1%
ERJ14N

AN +6V_IN → Vin+ (3)
AN +6V → Vin- (4)
OUT (1) → +6V_Analog_IMon
V+ (5) → SLO_AN +3.3V → C151 0.1µF 0805 → GND
GND (2) → GND
1000ma = 2.50V

INA194
50V/V

INA194AQDBVRQ1
SOT23-5

U34

Rs3
Rohm
0.200R ±1%
1210

DIG +6V_IN → Vin+ (3)
DIG +6V → Vin- (4)
OUT (1) → +6V_Dig_IMon
V+ (5) → SLO_AN +3.3V → C152 0.1µF 0805 → GND
GND (2) → GND
250ma = 2.50V

INA194
50V/V

INA194AQDBVRQ1
SOT23-5

U17

Rs1
Rohm
0.200R ±1%
1210

AN -6V → Vin+ (3)
AN -6V_IN → Vin- (4)
OUT (1) → -6V_Analog_IMon
V+ (5) → SLO_AN +3.3V
GND (2) → GND
250ma = 2.50V

INA194
50V/V

INA194AQDBVRQ1
SOT23-5

R65 6.04K ±1% 0603
R86 18K ±1% 0603
GND — C56 0.1µF 0603
AN +6V_IN → AN +6V_IN
+6V_Analog_VMon

R87 6.04K ±1% 0603
R88 18K ±1% 0603
GND — C70 0.1µF 0603
DIG +6V_IN → DIG +6V_IN
+6V_Dig_VMon

VREF 2.5V
R27 2K ±1% 0603
R64 15K ±1% 0603
AN -6V_IN → AN -6V_IN
-6V_Analog_VMon
C69 0.1µF 0603 — GND
D6 1N4148WX-TP SOD-323

T2K FEB64 - Voltage Regulators - Volt/Curr Monitor

Revision 2	Drawing # 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 3 of 16	Size: B	
	Drawn by: D. Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2- Regulators.SCHDOC			5:10:20 PM

JTAG pinout compatible with
Silicon Technologies
USB DEBUG ADAPTER

JTAG
HEADER 5X2
IDC10/RA

R67 10K ±1% 0603
R68 10K ±1% 0603
R73 10K ±1% 0603
R75 10K ±1% 0603
SLO +3.3V
GND
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI

U16
Analog Devices
ADM3072EARZ
8-SOIC
C78 0.1µF 0603
485_TX_EN
485_TXD
485_RXD
VCC
GND
MSCB_RS485A
MSCB_RS485B

U15
Silicon Laboratories
C8051F133-GQ
64-TQFP
C8051F131
C8051F133
TQFP-64
R50 10K ±1% 0603
CPU_NC0
CPU_NC1
CPU_RESETn
CPU_TDO
JTAG_TDI
JTAG_TCK
JTAG_TMS
SLO +3.3V
485_TXD
485_RXD
SMB_DAT
SMB_CLK
CHG_PMP_CLK
485_TX_EN
APD_DAC_CSn0
NC0
NC1
RSTn
TDO
TDI
TCK
TMS
VDD
DGND
TX0/P0.0
RX0/P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
CP1-
CP1+
CP0-
CP0+
AGND
AV+
Vref
Vref0
AIN0.0
AIN0.1
AIN0.2
AIN0.3
AIN0.4
AIN0.5
AIN0.6
AIN0.7
XTAL1
XTAL2
MONEN
P1.7/AIN2.7
P1.6/AIN2.6
P1.5/AIN2.5
P1.4/AIN2.4
P1.3/AIN2.3
P1.2/AIN2.2
P1.1/AIN2.1
P1.0/AIN2.0
P2.7
P2.6
P2.5
P0.7
P3.0
P3.1
P3.2
P3.3
P3.4
P3.5
P3.6
P3.7
P2.0
P2.1
P2.2
P2.3
P2.4
APD_DAC_CSn1
APD_DAC_CSn2
APD_DAC_CSn3
REG_Enable
SPARE4
SPARE5
APD_DAC_CSn4
SLO +3.3V
GND
APD_DAC_CSn5
RAM_CSn
RAM_WPn
SPI_MISO
RAM_HLDn
SPI_SCK
SPI_MOSI
R60 10K ±1% 0603

SLO_AN +3.3V
C79 0.1µF 0603
R66 4K7 ±1% 0603
R69 1.20K ±1% 0603
0.7Volts
SST_REF
SST_IO1
SST_IO2
VREF_2.4V
BiasVoltageReadback
BiasCurrentSense
+6V_Dig_VMon
+6V_Analog_VMon
-6V_Analog_VMon
-6V_Analog_IMon
+6V_Analog_IMon
+6V_Dig_IMon
C168 0.1µF 0603
C80 10000pF 0603
C103 0.1µF 0603

U45
Analog Devices
ADI7486AARMZ-REEL7
MSOP10
TD1 MMBT3904
TD2 MMBT3904
Cf2 100pF 0603
Cf3 100pF 0603
D1+
D1-
D2+
D2-
SST
ADD0
ADD1
RSVD
VCC
GND
SST_IO2
ADD = 0x48
+3.3V
C101 0.1µF 0603
R78 10K ±1% 0603
SST_DRV2
R79 10K ±1% 0603

U18
Analog Devices
ADI7486AARMZ-REEL7
MSOP10
Cf4 100pF 0603
Cf6 100pF 0603
Dcb2
De2
Dcb1
De1
SST_IO1
ADD = 0x48
C87 0.1µF 0603

U19
Analog Devices
ADI7486AARMZ-REEL7
MSOP10
Cf5 100pF 0603
Cf7 100pF 0603
Dcb4
De4
Dcb3
De3
SST_IO1
ADD = 0x49
C88 0.1µF 0603
R72 10K ±1% 0603
SST_DRV1
R74 10K ±1% 0603

U20
Analog Devices
ADI7486AARMZ-REEL7
MSOP10
Cf8 100pF 0603
Cf10 100pF 0603
Dcb6
De6
Dcb5
De5
SST_IO1
ADD = 0x4A
C91 0.1µF 0603

U21
Analog Devices
ADI7486AARMZ-REEL7
MSOP10
Cf9 100pF
Cf11 100pF
Dcb8
De8
Dcb7
De7
SST_IO1
ADD = 0x4B
C92 0.1µF 0603

PIN CONFIGURATION — SO, TSSOP

C81 0.1µF 0603
C82 0.1µF 0603
C83 0.1µF 0603

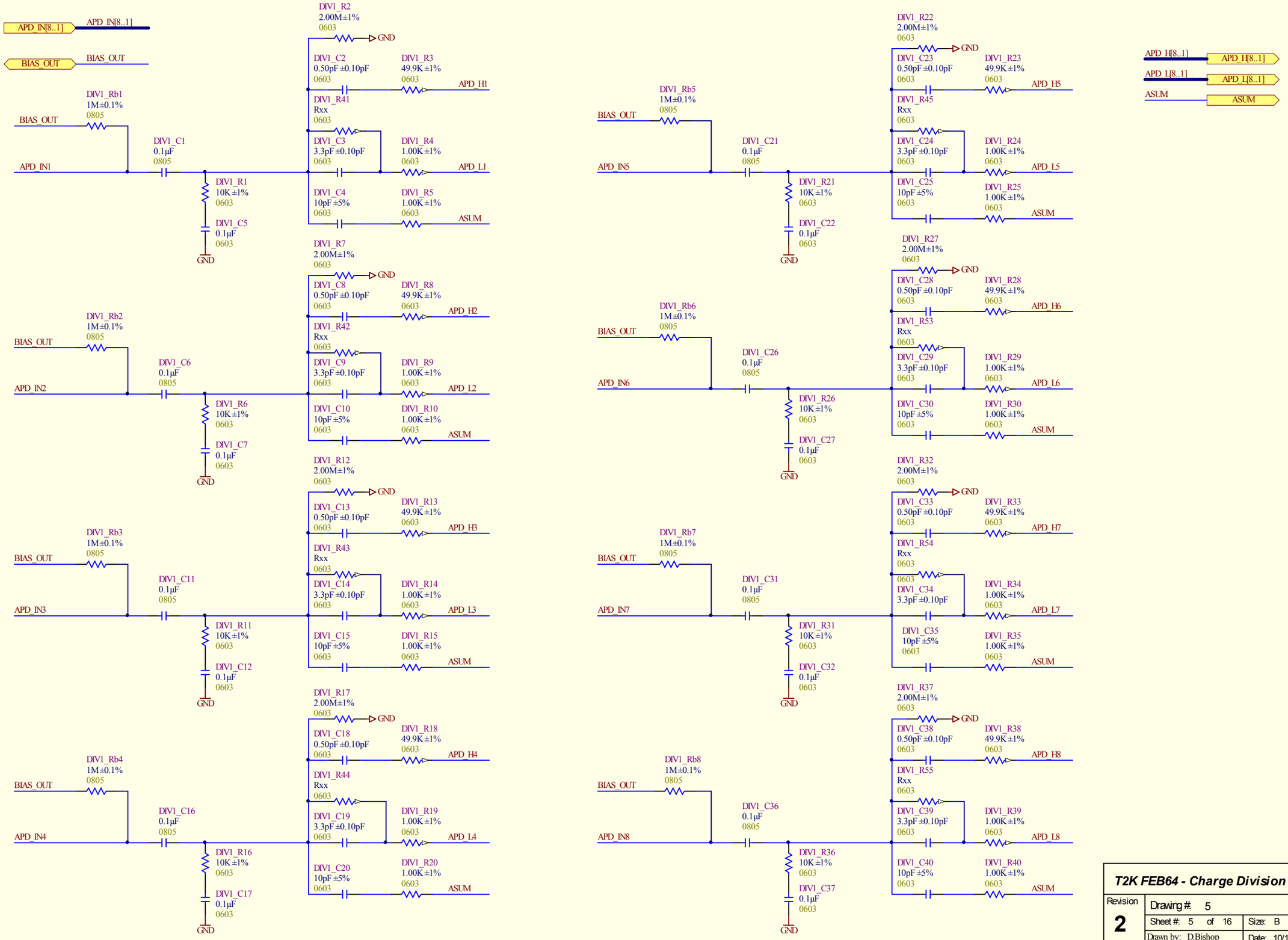
U40
Atmel
16K (2K x 8)
AT25160AN-10SU-2.7
8-SOIC
C161 0.1µF 0603
VCC
GND
SI
SO
SCK
CS
HOLD
WP
SPI_MOSI
SPI_MISO
SPI_SCK
RAM_CSn
RAM_HLDn
RAM_WPn

U12
NXP Semiconductors
PCA9539PW-T
TSSOP-24
C40 0.1µF 0603
Address 1110100
SMB_CLK
SMB_DAT
A1
A0
PIO_ResetN
RESET
INT
VDD
VSS
SCL
SDA
I/O1.7
I/O1.6
I/O1.5
I/O1.4
I/O1.3
I/O1.2
I/O1.1
I/O1.0
I/O0.6
I/O0.7
I/O0.5
I/O0.4
I/O0.3
I/O0.2
I/O0.1
I/O0.0
EN_BIASn4
EN_BIASn0
EN_BIASn6
EN_BIASn2
EN_BIASn5
EN_BIASn1
EN_BIASn7
EN_BIASn3
RP23 10K ±1% 0603 x 4
RP24 10K ±1% 0603 x 4
RP21 470R ±5% 0603 x 4
RP22 470R ±5% 0603 x 4
Backplane_Add7
Backplane_Add6
Backplane_Add5
Backplane_Add4
Backplane_Add3
Backplane_Add2
Backplane_Add1
Backplane_Add0

R70 4K7 ±1% 0603
R71 4K7 ±1% 0603
SMB_DAT
SMB_CLK
SPI_SCK
SPI_MOSI
APD_DAC_CSn[7..0]
SUM_DAC_CSn
DAC_ResetN
REG_Enable
ASUM_SYNC
ASUM_PdwnN
ASUM_TESTn
CHG_PMP_CLK
+6V_Analog_VMon
+6V_Analog_IMon
-6V_Analog_VMon
-6V_Analog_IMon
+6V_Dig_VMon
+6V_Dig_IMon
BiasCurrentSense
BiasVoltageReadback
Df[8..1]
Dcb[8..1]
CPU_TDO
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
EN_BIASn[7..0]
Backplane_Add[7..0]

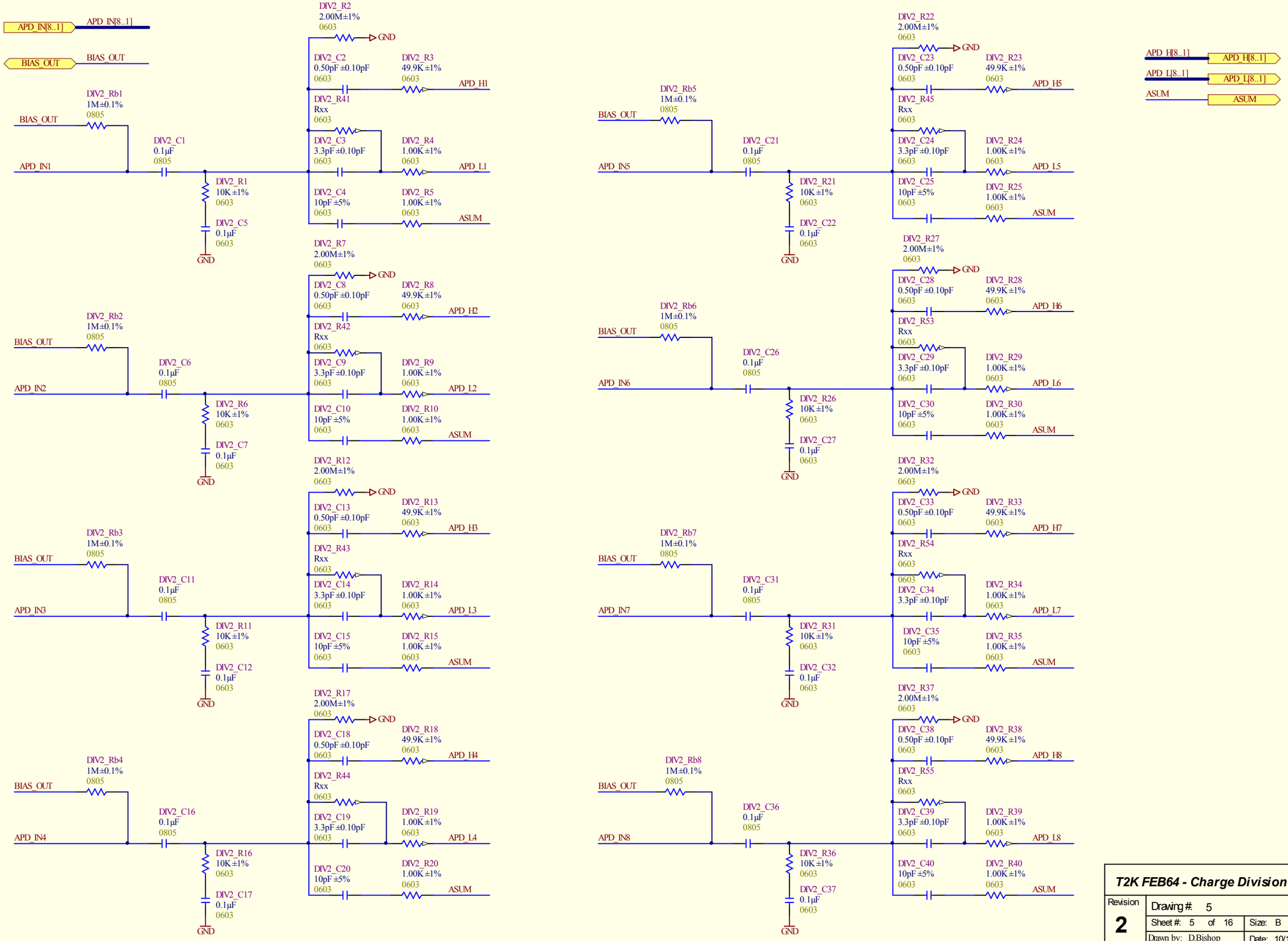
T2K FEB64 - MIDAS Slow Control

Revision	Drawing #	4		
2	Sheet # 4 of 16	Size: B	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
	Drawn by: D. Bishop	Date: 10/12/2008		
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Slow Control.SCHDOC				5:10:20 PM



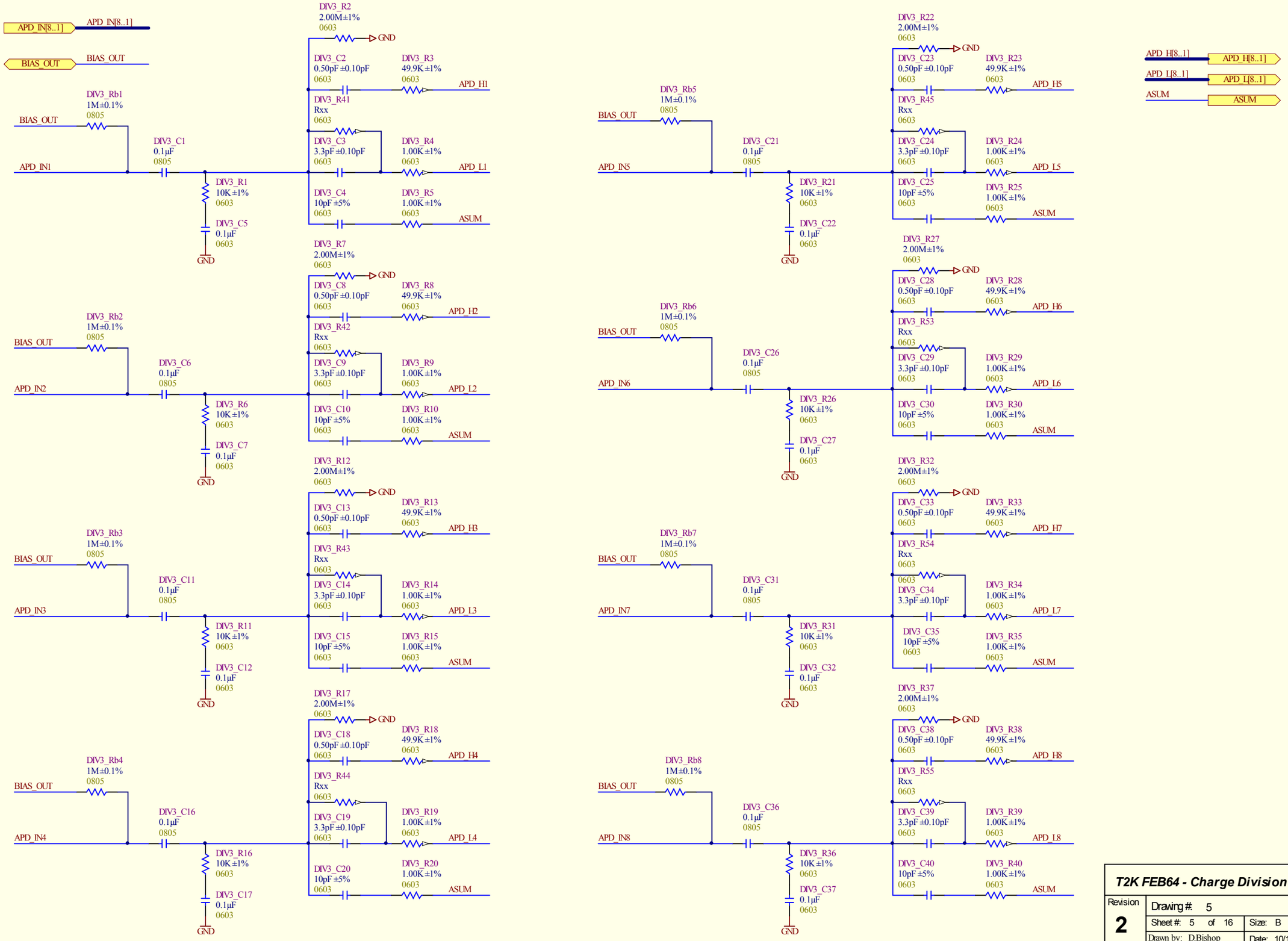
T2K FEB64 - Charge Division

Revision 2	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Charge Division.SCHDOC			5:10:20 PM



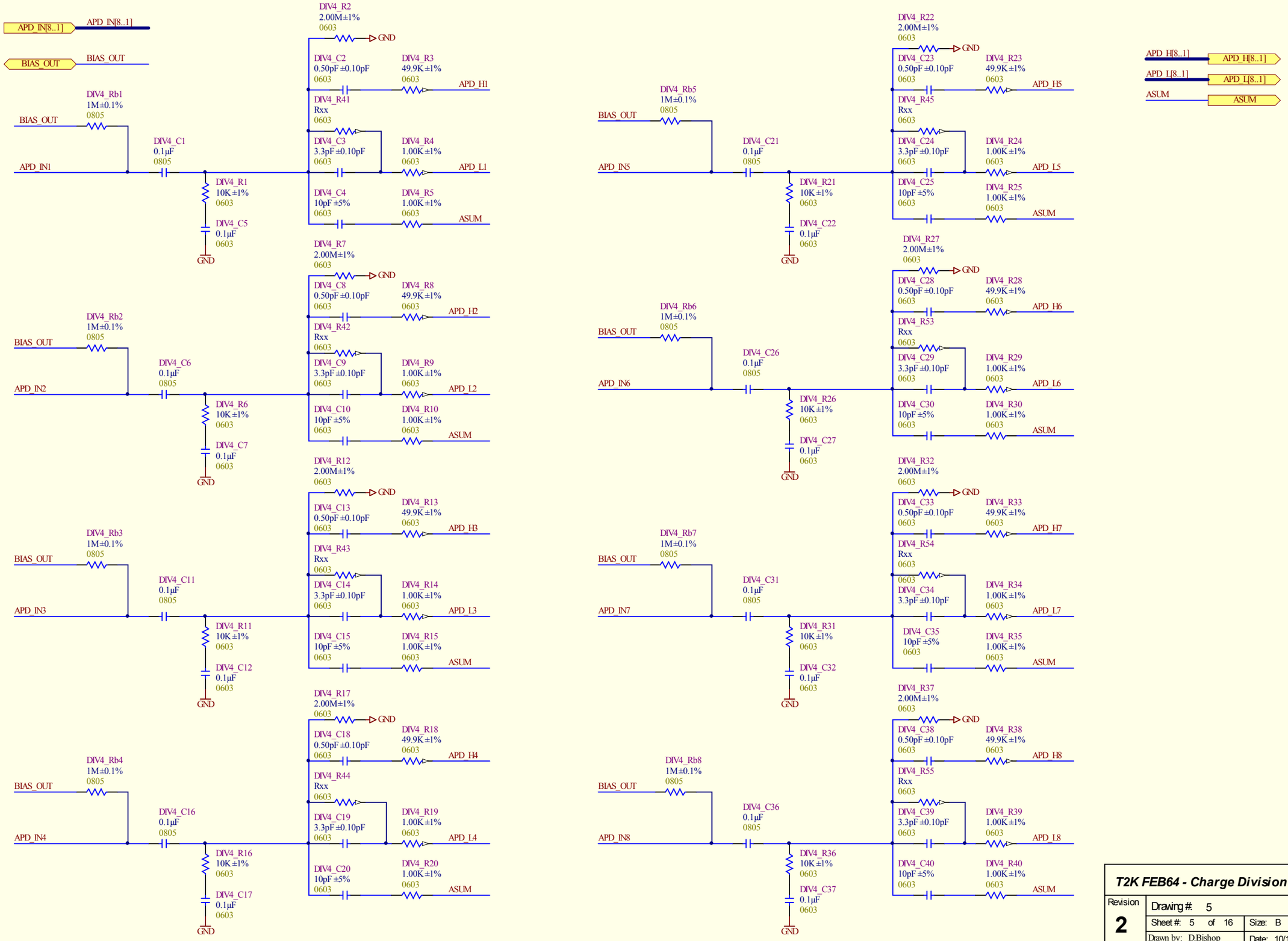
T2K FEB64 - Charge Division

Revision 2	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Charge Division.SCHDOC			5:10:21 PM



T2K FEB64 - Charge Division

Revision 2	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Charge Division.SCHDOC			5:10:21 PM


APD_IN[8..1]
APD_IN[8..1]
BIAS_OUT
BIAS_OUT
DIV4_Rb1
1M±0.1%
0805
BIAS_OUT
APD_IN1
DIV4_C1
0.1µF
0805
DIV4_R1
10K±1%
0603
DIV4_C5
0.1µF
0603
GND
DIV4_R2
2.00M±1%
0603
GND
DIV4_C2
0.50pF±0.10pF
0603
DIV4_R3
49.9K±1%
0603
APD_H1
DIV4_R41
Rxx
0603
DIV4_C3
3.3pF±0.10pF
0603
DIV4_R4
1.00K±1%
0603
APD_L1
DIV4_C4
10pF±5%
0603
DIV4_R5
1.00K±1%
0603
ASUM
DIV4_Rb2
1M±0.1%
0805
BIAS_OUT
APD_IN2
DIV4_C6
0.1µF
0805
DIV4_R6
10K±1%
0603
DIV4_C7
0.1µF
0603
GND
DIV4_R7
2.00M±1%
0603
GND
DIV4_C8
0.50pF±0.10pF
0603
DIV4_R8
49.9K±1%
0603
APD_H2
DIV4_R42
Rxx
0603
DIV4_C9
3.3pF±0.10pF
0603
DIV4_R9
1.00K±1%
0603
APD_L2
DIV4_C10
10pF±5%
0603
DIV4_R10
1.00K±1%
0603
ASUM
DIV4_Rb3
1M±0.1%
0805
BIAS_OUT
APD_IN3
DIV4_C11
0.1µF
0805
DIV4_R11
10K±1%
0603
DIV4_C12
0.1µF
0603
GND
DIV4_R12
2.00M±1%
0603
GND
DIV4_C13
0.50pF±0.10pF
0603
DIV4_R13
49.9K±1%
0603
APD_H3
DIV4_R43
Rxx
0603
DIV4_C14
3.3pF±0.10pF
0603
DIV4_R14
1.00K±1%
0603
APD_L3
DIV4_C15
10pF±5%
0603
DIV4_R15
1.00K±1%
0603
ASUM
DIV4_Rb4
1M±0.1%
0805
BIAS_OUT
APD_IN4
DIV4_C16
0.1µF
0805
DIV4_R16
10K±1%
0603
DIV4_C17
0.1µF
0603
GND
DIV4_R17
2.00M±1%
0603
GND
DIV4_C18
0.50pF±0.10pF
0603
DIV4_R18
49.9K±1%
0603
APD_H4
DIV4_R44
Rxx
0603
DIV4_C19
3.3pF±0.10pF
0603
DIV4_R19
1.00K±1%
0603
APD_L4
DIV4_C20
10pF±5%
0603
DIV4_R20
1.00K±1%
0603
ASUM
DIV4_Rb5
1M±0.1%
0805
BIAS_OUT
APD_IN5
DIV4_C21
0.1µF
0805
DIV4_R21
10K±1%
0603
DIV4_C22
0.1µF
0603
GND
DIV4_R22
2.00M±1%
0603
GND
DIV4_C23
0.50pF±0.10pF
0603
DIV4_R23
49.9K±1%
0603
APD_H5
DIV4_R45
Rxx
0603
DIV4_C24
3.3pF±0.10pF
0603
DIV4_R24
1.00K±1%
0603
APD_L5
DIV4_C25
10pF±5%
0603
DIV4_R25
1.00K±1%
0603
ASUM
DIV4_Rb6
1M±0.1%
0805
BIAS_OUT
APD_IN6
DIV4_C26
0.1µF
0805
DIV4_R26
10K±1%
0603
DIV4_C27
0.1µF
0603
GND
DIV4_R27
2.00M±1%
0603
GND
DIV4_C28
0.50pF±0.10pF
0603
DIV4_R28
49.9K±1%
0603
APD_H6
DIV4_R53
Rxx
0603
DIV4_C29
3.3pF±0.10pF
0603
DIV4_R29
1.00K±1%
0603
APD_L6
DIV4_C30
10pF±5%
0603
DIV4_R30
1.00K±1%
0603
ASUM
DIV4_Rb7
1M±0.1%
0805
BIAS_OUT
APD_IN7
DIV4_C31
0.1µF
0805
DIV4_R31
10K±1%
0603
DIV4_C32
0.1µF
0603
GND
DIV4_R32
2.00M±1%
0603
GND
DIV4_C33
0.50pF±0.10pF
0603
DIV4_R33
49.9K±1%
0603
APD_H7
DIV4_R54
Rxx
0603
0603
DIV4_C34
3.3pF±0.10pF
DIV4_R34
1.00K±1%
0603
APD_L7
DIV4_C35
10pF±5%
0603
DIV4_R35
1.00K±1%
0603
ASUM
DIV4_Rb8
1M±0.1%
0805
BIAS_OUT
APD_IN8
DIV4_C36
0.1µF
0805
DIV4_R36
10K±1%
0603
DIV4_C37
0.1µF
0603
GND
DIV4_R37
2.00M±1%
0603
GND
DIV4_C38
0.50pF±0.10pF
0603
DIV4_R38
49.9K±1%
0603
APD_H8
DIV4_R55
Rxx
0603
DIV4_C39
3.3pF±0.10pF
0603
DIV4_R39
1.00K±1%
0603
APD_L8
DIV4_C40
10pF±5%
0603
DIV4_R40
1.00K±1%
0603
ASUM
APD_H[8..1]
APD_H[8..1]
APD_L[8..1]
APD_L[8..1]
ASUM
ASUM
T2K FEB64 - Charge Division
Revision
2
Drawing #: 5
Sheet #: 5 of 16
Size: B
Drawn by: D.Bishop
Date: 10/12/2008
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Charge Division.SCHDOC
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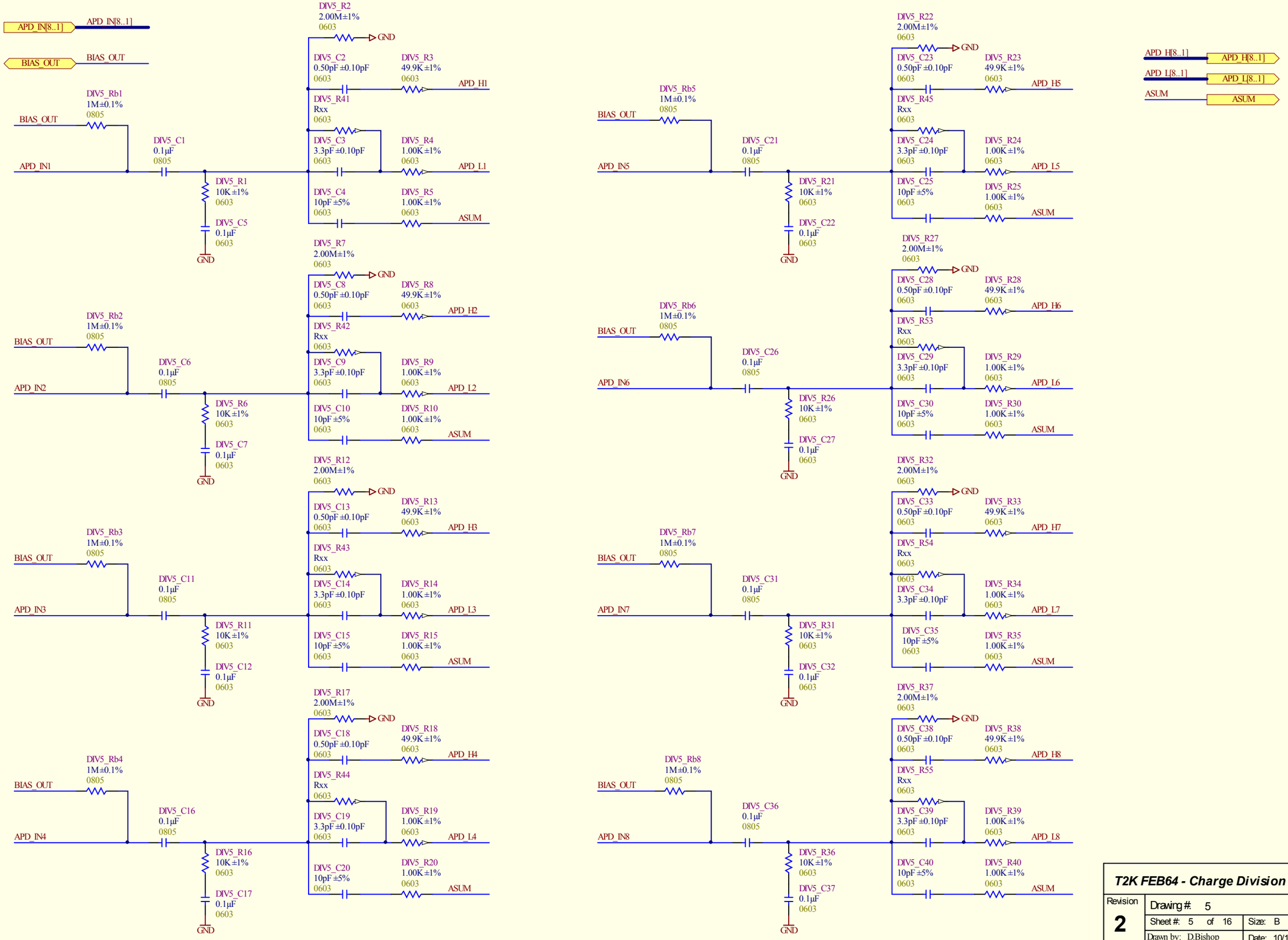
APD_IN[8..1]
APD_IN[8..1]
BIAS_OUT
BIAS_OUT
DIV5_Rb1
1M±0.1%
0805
BIAS_OUT
APD_IN1
DIV5_C1
0.1µF
0805
DIV5_R1
10K±1%
0603
DIV5_C5
0.1µF
0603
GND
DIV5_R2
2.00M±1%
0603
GND
DIV5_C2
0.50pF±0.10pF
0603
DIV5_R3
49.9K±1%
0603
APD_H1
DIV5_R41
Rxx
0603
DIV5_C3
3.3pF±0.10pF
0603
DIV5_R4
1.00K±1%
0603
APD_L1
DIV5_C4
10pF±5%
0603
DIV5_R5
1.00K±1%
0603
ASUM
DIV5_Rb2
1M±0.1%
0805
BIAS_OUT
APD_IN2
DIV5_C6
0.1µF
0805
DIV5_R6
10K±1%
0603
DIV5_C7
0.1µF
0603
GND
DIV5_R7
2.00M±1%
0603
GND
DIV5_C8
0.50pF±0.10pF
0603
DIV5_R8
49.9K±1%
0603
APD_H2
DIV5_R42
Rxx
0603
DIV5_C9
3.3pF±0.10pF
0603
DIV5_R9
1.00K±1%
0603
APD_L2
DIV5_C10
10pF±5%
0603
DIV5_R10
1.00K±1%
0603
ASUM
DIV5_Rb3
1M±0.1%
0805
BIAS_OUT
APD_IN3
DIV5_C11
0.1µF
0805
DIV5_R11
10K±1%
0603
DIV5_C12
0.1µF
0603
GND
DIV5_R12
2.00M±1%
0603
GND
DIV5_C13
0.50pF±0.10pF
0603
DIV5_R13
49.9K±1%
0603
APD_H3
DIV5_R43
Rxx
0603
DIV5_C14
3.3pF±0.10pF
0603
DIV5_R14
1.00K±1%
0603
APD_L3
DIV5_C15
10pF±5%
0603
DIV5_R15
1.00K±1%
0603
ASUM
DIV5_Rb4
1M±0.1%
0805
BIAS_OUT
APD_IN4
DIV5_C16
0.1µF
0805
DIV5_R16
10K±1%
0603
DIV5_C17
0.1µF
0603
GND
DIV5_R17
2.00M±1%
0603
GND
DIV5_C18
0.50pF±0.10pF
0603
DIV5_R18
49.9K±1%
0603
APD_H4
DIV5_R44
Rxx
0603
DIV5_C19
3.3pF±0.10pF
0603
DIV5_R19
1.00K±1%
0603
APD_L4
DIV5_C20
10pF±5%
0603
DIV5_R20
1.00K±1%
0603
ASUM
DIV5_Rb5
1M±0.1%
0805
BIAS_OUT
APD_IN5
DIV5_C21
0.1µF
0805
DIV5_R21
10K±1%
0603
DIV5_C22
0.1µF
0603
GND
DIV5_R22
2.00M±1%
0603
GND
DIV5_C23
0.50pF±0.10pF
0603
DIV5_R23
49.9K±1%
0603
APD_H5
DIV5_R45
Rxx
0603
DIV5_C24
3.3pF±0.10pF
0603
DIV5_R24
1.00K±1%
0603
APD_L5
DIV5_C25
10pF±5%
0603
DIV5_R25
1.00K±1%
0603
ASUM
DIV5_Rb6
1M±0.1%
0805
BIAS_OUT
APD_IN6
DIV5_C26
0.1µF
0805
DIV5_R26
10K±1%
0603
DIV5_C27
0.1µF
0603
GND
DIV5_R27
2.00M±1%
0603
GND
DIV5_C28
0.50pF±0.10pF
0603
DIV5_R28
49.9K±1%
0603
APD_H6
DIV5_R53
Rxx
0603
DIV5_C29
3.3pF±0.10pF
0603
DIV5_R29
1.00K±1%
0603
APD_L6
DIV5_C30
10pF±5%
0603
DIV5_R30
1.00K±1%
0603
ASUM
DIV5_Rb7
1M±0.1%
0805
BIAS_OUT
APD_IN7
DIV5_C31
0.1µF
0805
DIV5_R31
10K±1%
0603
DIV5_C32
0.1µF
0603
GND
DIV5_R32
2.00M±1%
0603
GND
DIV5_C33
0.50pF±0.10pF
0603
DIV5_R33
49.9K±1%
0603
APD_H7
DIV5_R54
Rxx
0603
0603
DIV5_C34
3.3pF±0.10pF
DIV5_R34
1.00K±1%
0603
APD_L7
DIV5_C35
10pF±5%
0603
DIV5_R35
1.00K±1%
0603
ASUM
DIV5_Rb8
1M±0.1%
0805
BIAS_OUT
APD_IN8
DIV5_C36
0.1µF
0805
DIV5_R36
10K±1%
0603
DIV5_C37
0.1µF
0603
GND
DIV5_R37
2.00M±1%
0603
GND
DIV5_C38
0.50pF±0.10pF
0603
DIV5_R38
49.9K±1%
0603
APD_H8
DIV5_R55
Rxx
0603
DIV5_C39
3.3pF±0.10pF
0603
DIV5_R39
1.00K±1%
0603
APD_L8
DIV5_C40
10pF±5%
0603
DIV5_R40
1.00K±1%
0603
ASUM
APD_H[8..1]
APD_H[8..1]
APD_L[8..1]
APD_L[8..1]
ASUM
ASUM
T2K FEB64 - Charge Division
Revision
2
Drawing #: 5
Sheet #: 5 of 16
Size: B
Drawn by: D.Bishop
Date: 10/12/2008
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Charge Division.SCHDOC
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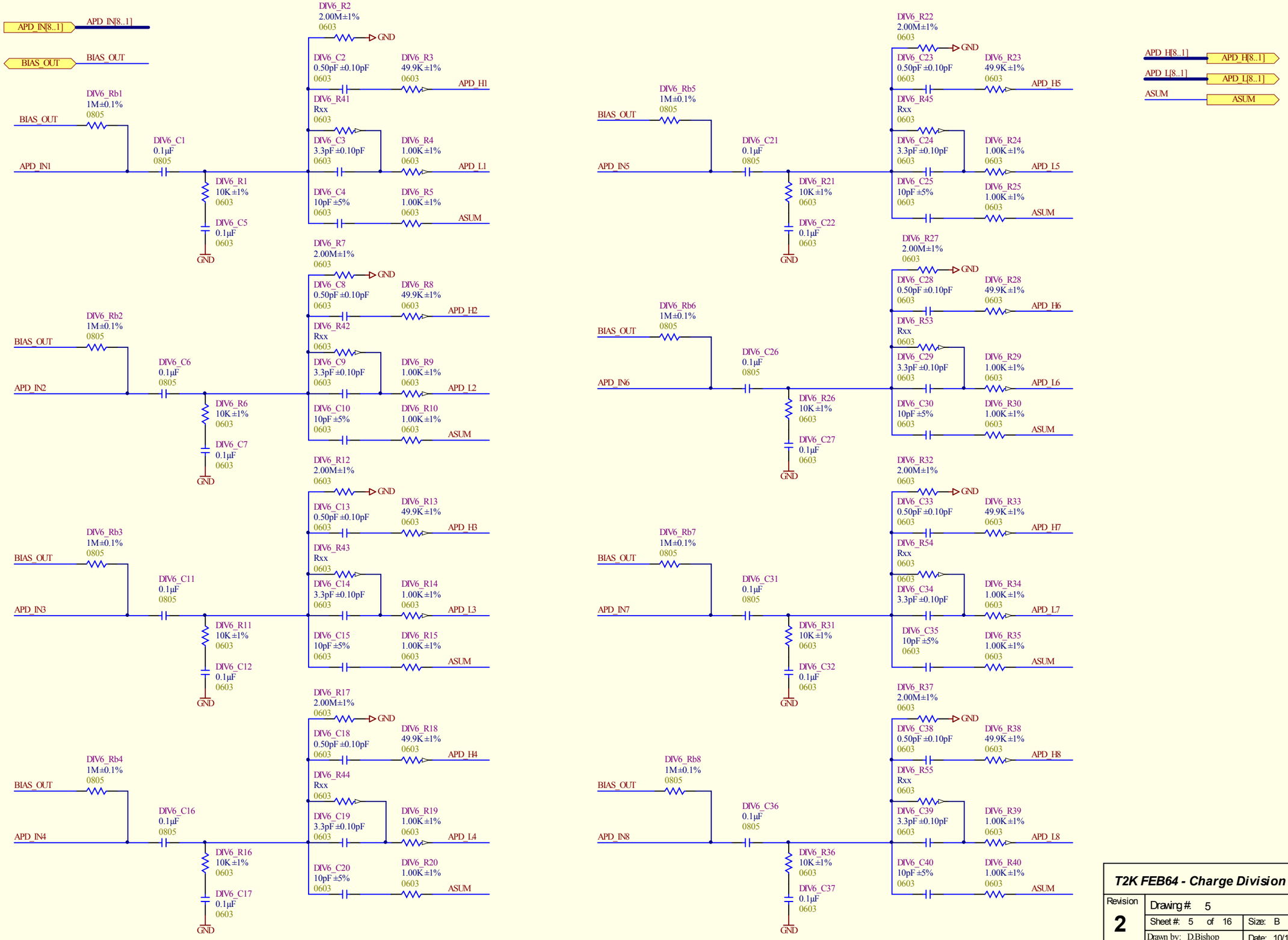

T2K FEB64 - Charge Division

Revision 2	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
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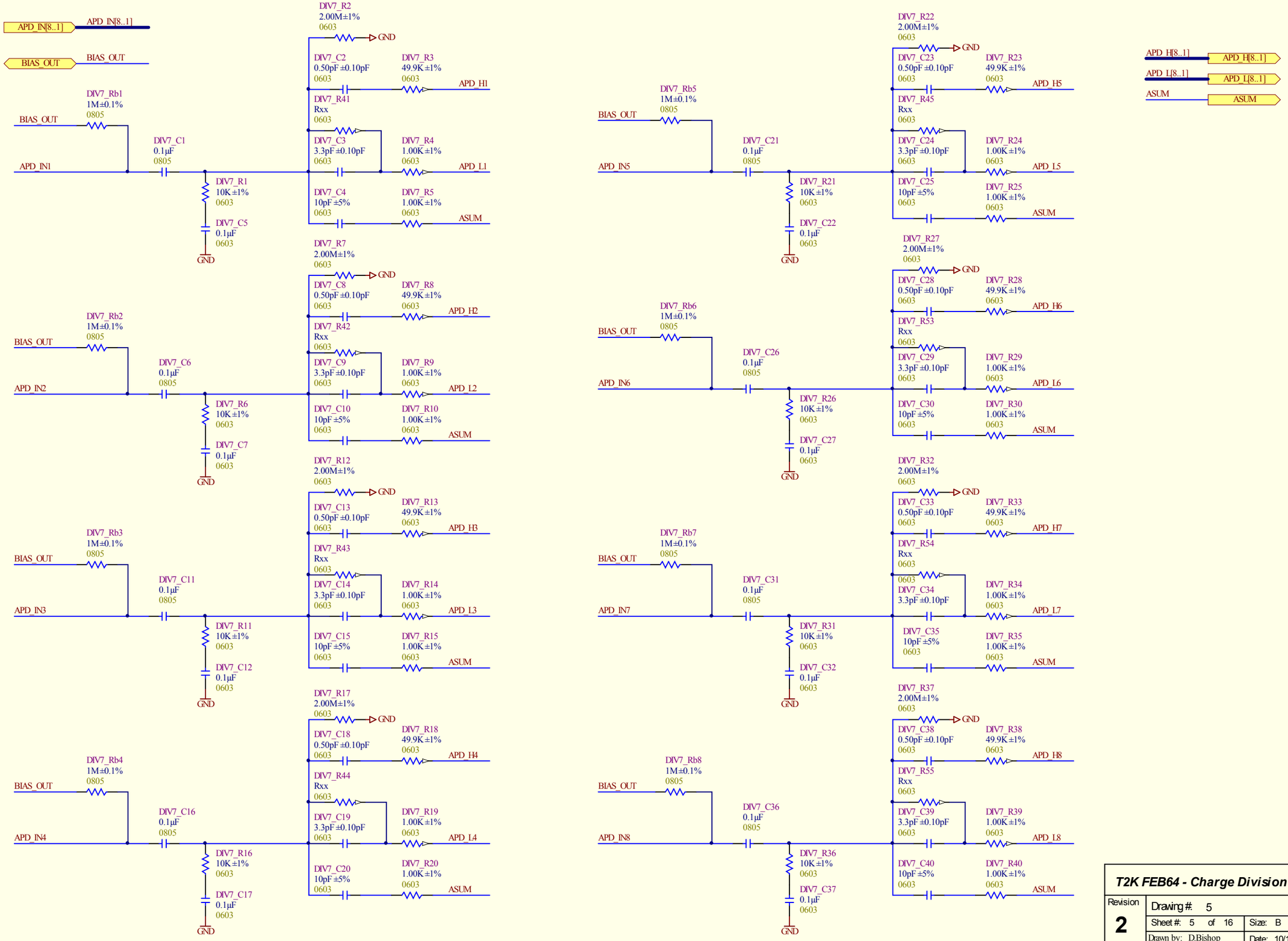

T2K FEB64 - Charge Division

Revision 2	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
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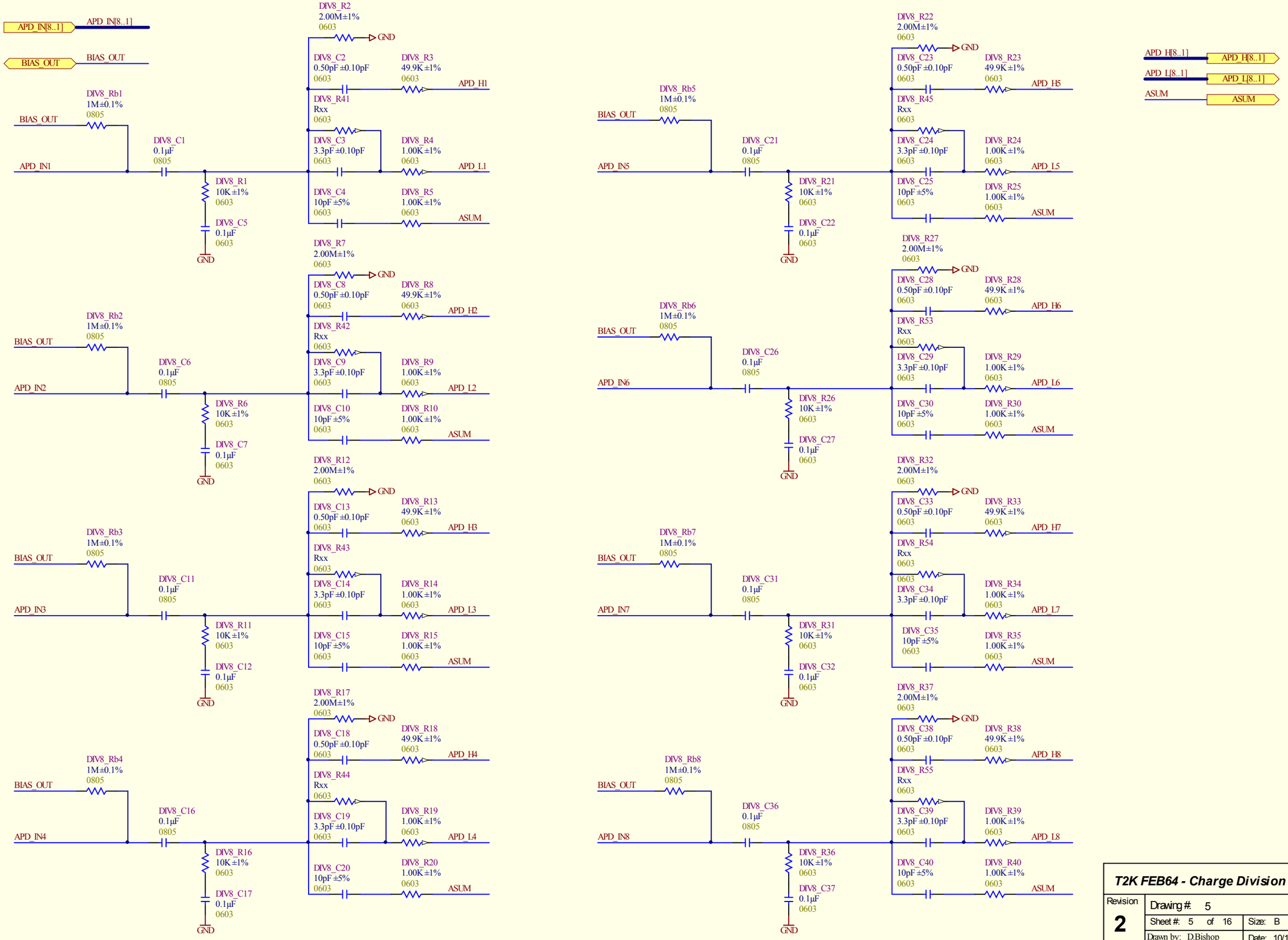


T2K FEB64 - Charge Division

Revision 2	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Charge Division.SCHDOC			5:10:22 PM

BIAS_SW

T2K FEB_Rev2 - 8 Channel MOSFET Switch.SCHDOC

EN_BIASn[7..0] → EN_BIASn[7..0]
BIAS → BIAS
BIAS_SW[7..0] ← BIAS_SW[7..0]

I1
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW0 → BIAS_SW
BIAS_OUT → BIAS_OUT0
BiasCurrentSense → IBIAS_RDBK1
BiasVoltageReadback → VBIAS_RDBK1

I2
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW1 → BIAS_SW
BIAS_OUT → BIAS_OUT1
BiasCurrentSense → IBIAS_RDBK2
BiasVoltageReadback → VBIAS_RDBK2

I3
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW2 → BIAS_SW
BIAS_OUT → BIAS_OUT2
BiasCurrentSense → IBIAS_RDBK3
BiasVoltageReadback → VBIAS_RDBK3

I4
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW3 → BIAS_SW
BIAS_OUT → BIAS_OUT3
BiasCurrentSense → IBIAS_RDBK4
BiasVoltageReadback → VBIAS_RDBK4

I5
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW4 → BIAS_SW
BIAS_OUT → BIAS_OUT4
BiasCurrentSense → IBIAS_RDBK5
BiasVoltageReadback → VBIAS_RDBK5

I6
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW5 → BIAS_SW
BIAS_OUT → BIAS_OUT5
BiasCurrentSense → IBIAS_RDBK6
BiasVoltageReadback → VBIAS_RDBK6

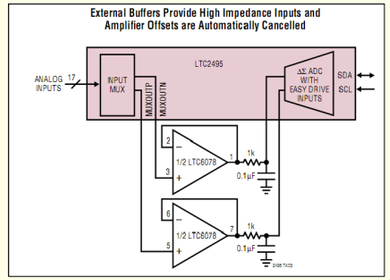
I7
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW6 → BIAS_SW
BIAS_OUT → BIAS_OUT6
BiasCurrentSense → IBIAS_RDBK7
BiasVoltageReadback → VBIAS_RDBK7

I8
T2K FEB_Rev2 - BIAS Current Sense.SchDoc
BIAS_SW7 → BIAS_SW
BIAS_OUT → BIAS_OUT7
BiasCurrentSense → IBIAS_RDBK8
BiasVoltageReadback → VBIAS_RDBK8

BIAS_OUT[7..0] → BIAS_OUT[7..0]

Table 5a. Performance vs Gain in Normal Speed Mode (V_{CC} = 5V, V_{REF} = 5V)

GAIN	1	4	8	16	32	64	128	256	UNIT
Input Span	±2.5	±0.625	±0.312	±0.156	±78m	±39m	±19.5m	±9.76m	V
LSB	38.1	9.54	4.77	2.38	1.19	0.595	0.298	0.149	µV
Noise Free Resolution*	65536	65536	65536	65536	65536	65536	32768	16384	Counts
Gain Error	5	5	5	5	5	5	5	8	ppm of FS
Offset Error	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	µV



Vref1
Analog Devices Inc
REF192FSZ
2.5V ±0.2%

SLO_AN_+3.3V → NC_TP1 (1)
VCC (2)
SLEEP (3)
GND (4)
NC (8)
NC (7)
OUT (6) → VREF_2.5V → VREF_2.5V
NC_TP5 (5)
C75 0.1µF 0603 → GND
C76 1.0µF 0603 → GND
8-SOIC

U43
Texas Instruments
INA326EA/2K5

R51 200K ±0.1% 0603 → RG (1)
RG (8)
MUXOUTp → IN+ (3)
GND → IN- (2)
GND → -V (4)
+V (7) ← SLO_AN_+3.3V
C97 0.1µF 0603 → GND
OUT (6) → R52 1.00K ±1% 0603 → ADCINp
REF (5) → 1.25V_Offset
C98 0.1µF 0603 → GND
VREF_2.5V → R61 200K ±0.1% 0603
R62 200K ±0.1% 0603 → GND
C77 470pF 0603 → GND
8-MSOP

U44
AD8541ARTZ-REEL7
SOT235

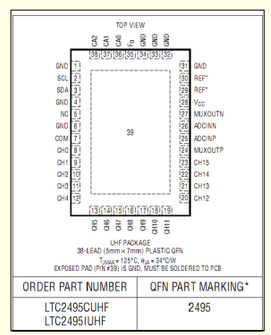
SLO_AN_+3.3V → C99 0.1µF 0603 → GND
MUXOUTn → V+ (3)
V- (4) → GND
OUT (1) → R63 1.00K ±1% 0603 → ADCINn
C100 0.1µF 0603 → GND

ADC1
Linear Technologies
LTC2495IUHF#PBF

IBIAS_RDBK2 (8) → CH0
IBIAS_RDBK4 (9) → CH1
IBIAS_RDBK6 (10) → CH2
IBIAS_RDBK8 (11) → CH3
VBIAS_RDBK8 (12) → CH4
VBIAS_RDBK6 (13) → CH5
VBIAS_RDBK4 (14) → CH6
VBIAS_RDBK2 (15) → CH7
IBIAS_RDBK1 (16) → CH8
IBIAS_RDBK3 (17) → CH9
IBIAS_RDBK5 (18) → CH10
IBIAS_RDBK7 (19) → CH11
VBIAS_RDBK7 (20) → CH12
VBIAS_RDBK5 (21) → CH13
VBIAS_RDBK3 (22) → CH14
VBIAS_RDBK1 (23) → CH15
ADC_COM (7) → COM
REF+ (29) ← VREF_2.5V
REF- (30) → GND
MUXOUTP (24) ← MUXOUTp
ADCINp (25) ← ADCINp
MUXOUTN (27) ← MUXOUTn
ADCINn (26) ← ADCINn
SCL (2) → SMB_CLK
SDA (3) → SMB_DAT
CA2 (38)
CA1 (37)
CA0 (36)
ADD = 1000101
FO (35) → GND
NC (5)
VCC (28) ← SLO_AN_+3.3V
C73 0.1µF 0603 → GND
C74 1.0µF 0603 → GND
GND (1, 4, 6, 31, 32, 33, 34, 39)
PP_GND
38-QFN

NOTE:
LTC2495 requires CMOS level digital inputs (0.7xVCC min)

Rr1 10K ±0.1% 0603 ← VREF_2.5V
ADC_COM
Cr1 0.1µF 0603 → GND
Rr2 10K ±0.1% 0603 → GND



ORDER PART NUMBER	QFN PART MARKING*
LTC2495CUHF LTC2495IUHF	2495

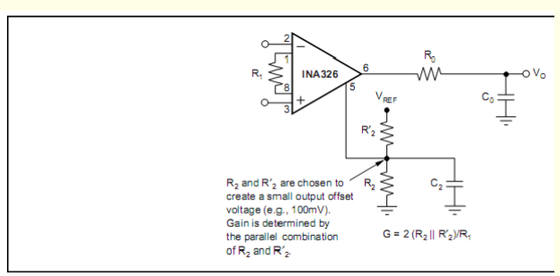
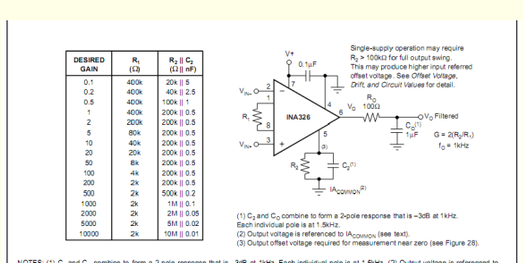


FIGURE 6. Generating Output Offset Voltage.

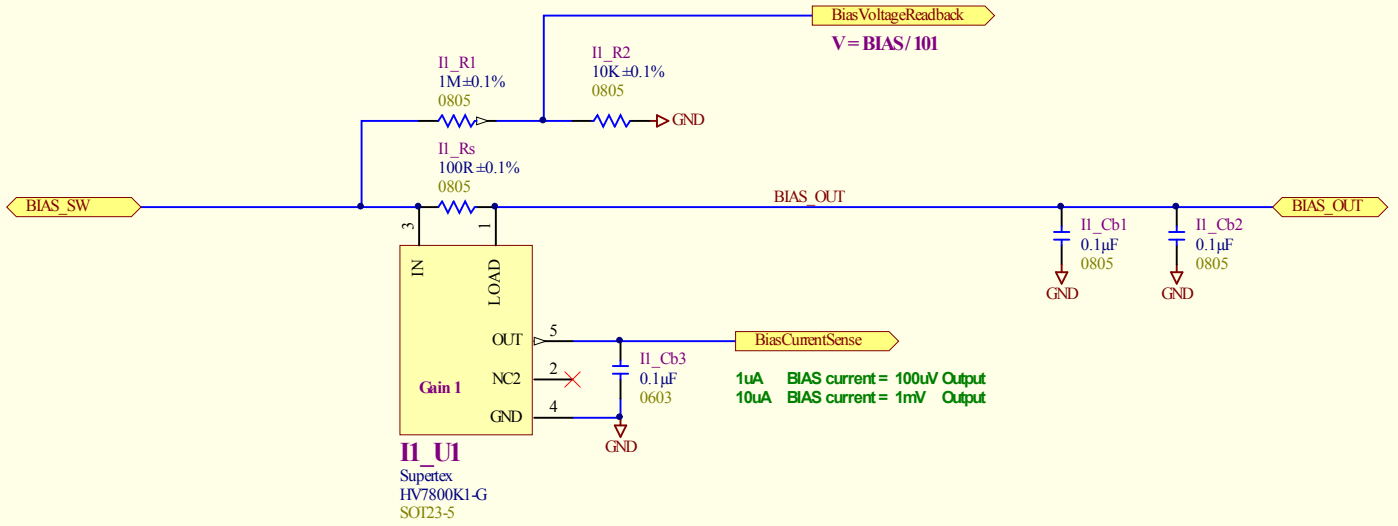


NOTES: (1) C_2 and C_O combine to form a 2-pole response that is –3dB at 1kHz. Each individual pole is at 1.5kHz. (2) Output voltage is referenced to $I_{A_{COMMON}}$ (see text). (3) Output offset voltage required for measurement near zero (see Figure 6).

FIGURE 1. Basic Connections. NOTE: Connections for INA327 differ—see Pin Configuration for detail.

T2K FEB64 - BIAS Output x 64 / Voltage & Current Readback

Revision	Drawing #: 6		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
2	Sheet #: 6 of 16	Size: B		
	Drawn by: D.Bishop	Date: 10/12/2008		
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - BIAS Output.SchDoc				5:10:22 PM



Electrical Characteristics (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units		Conditions
Supply							
V_{IN}	Supply voltage	8.0	-	450	V	*	---
I_Q	Quiescent supply current	-	-	50	µA	-	V_{IN} = 8V to 450V, V_{SENSE} = 0mV
Input and Output							
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	-	---
V_{OUT}	Output voltage	0	-	15	mV	-	V_{SENSE} = 0mV
		79	-	121		-	V_{SENSE} = 100mV
		177	-	223		-	V_{SENSE} = 200mV
		470	-	530		-	V_{SENSE} = 500mV
Dynamic Characteristics							
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	µs	-	V_{SENSE} step 5mV to 500mV
		-	-	2.0		-	V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	µs	-	V_{SENSE} step 500mV to 0mV

Notes: 1. Referenced to GND
2. $V_{SENSE} = V_{IN} - V_{LOAD}$
Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

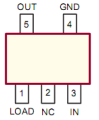
•G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



5-Lead SOT-23
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} [1]	-0.5V to +450V
V_{OUT} [1]	-0.5V to +10V
V_{SENSE} [2]	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
= "Green" Packaging

5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing # 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet # 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

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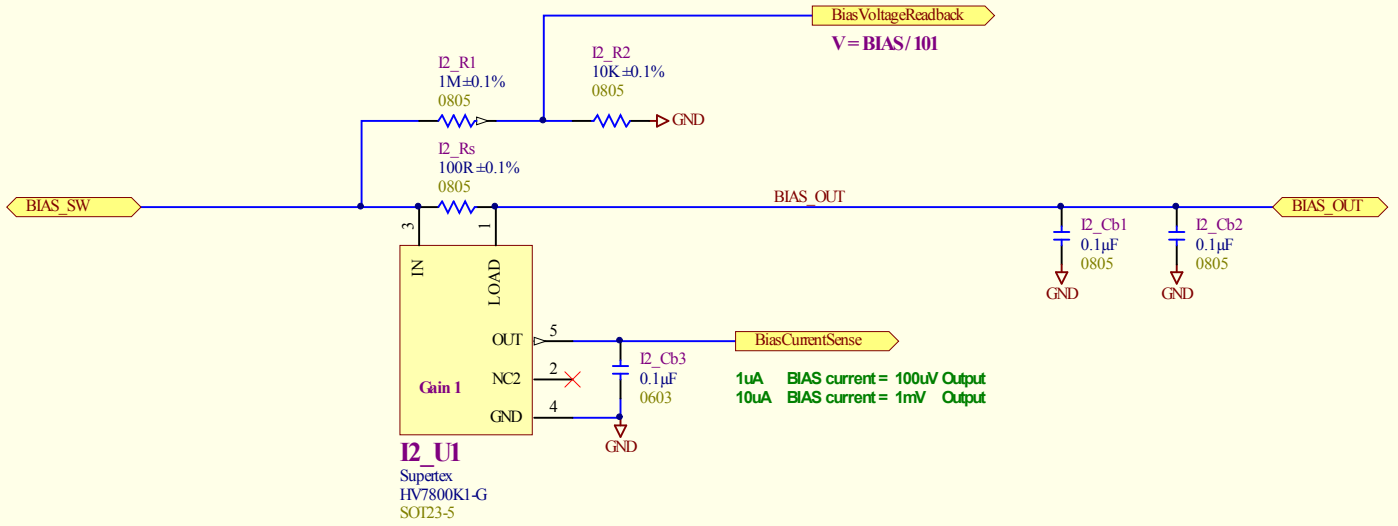

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units		Conditions
Supply							
V_{IN}	Supply voltage	8.0	-	450	V	*	---
I_Q	Quiescent supply current	-	-	50	µA	-	V_{IN} = 8V to 450V, V_{SENSE} = 0mV
Input and Output							
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	-	---
V_{OUT}	Output voltage	0	-	15	mV	-	V_{SENSE} = 0mV
		79	-	121		-	V_{SENSE} = 100mV
		177	-	223		-	V_{SENSE} = 200mV
		470	-	530		-	V_{SENSE} = 500mV
Dynamic Characteristics							
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	µs	-	V_{SENSE} step 5mV to 500mV
		-	-	2.0		-	V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	µs	-	V_{SENSE} step 500mV to 0mV

Notes: 1. Referenced to GND
2. $V_{SENSE} = V_{IN} - V_{LOAD}$
Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

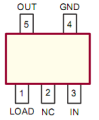
•G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



5-Lead SOT-23
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} [1]	-0.5V to +450V
V_{OUT} [1]	-0.5V to +10V
V_{SENSE} [2]	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Y = Last Digit of Year Sealed
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= "Green" Packaging

5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

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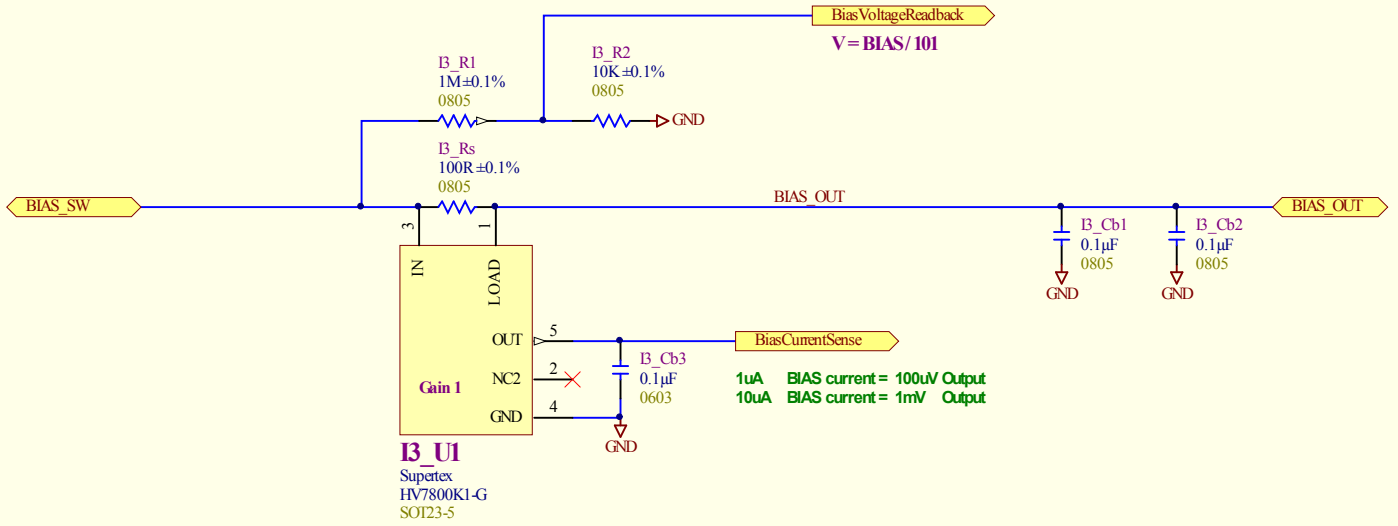

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units		Conditions
Supply							
V_{IN}	Supply voltage	8.0	-	450	V	*	---
I_Q	Quiescent supply current	-	-	50	µA	-	V_{IN} = 8V to 450V, V_{SENSE} = 0mV
Input and Output							
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	-	---
V_{OUT}	Output voltage	0	-	15	mV	-	V_{SENSE} = 0mV
		79	-	121		-	V_{SENSE} = 100mV
		177	-	223		-	V_{SENSE} = 200mV
		470	-	530		-	V_{SENSE} = 500mV
Dynamic Characteristics							
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	µs	-	V_{SENSE} step 5mV to 500mV
		-	-	2.0		-	V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	µs	-	V_{SENSE} step 500mV to 0mV

Notes: 1. Referenced to GND
2. $V_{SENSE} = V_{IN} - V_{LOAD}$
Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

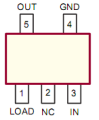
•G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



5-Lead SOT-23
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} [1]	-0.5V to +450V
V_{OUT} [1]	-0.5V to +10V
V_{SENSE} [2]	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

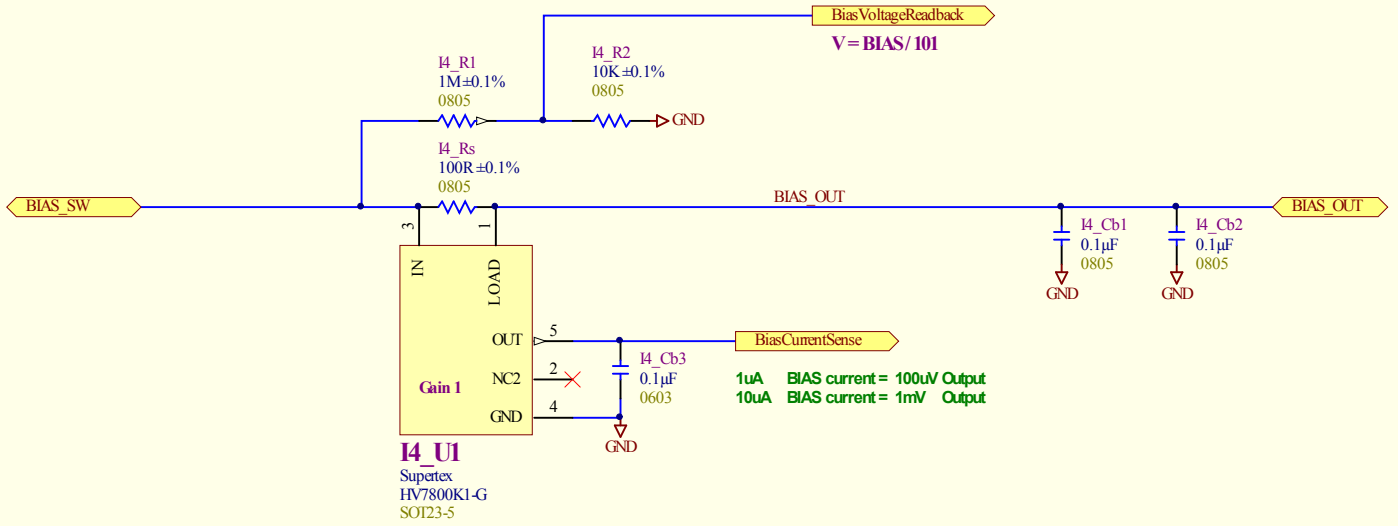
Y = Last Digit of Year Sealed
W = Code for Week Sealed
= "Green" Packaging

5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - BIAS Current Sense.SchDoc 5:10:23 PM



Electrical Characteristics (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units		Conditions
Supply							
V_{IN}	Supply voltage	8.0	-	450	V	*	---
I_Q	Quiescent supply current	-	-	50	µA	-	V_{IN} = 8V to 450V, V_{SENSE} = 0mV
Input and Output							
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	-	---
V_{OUT}	Output voltage	0	-	15	mV	-	V_{SENSE} = 0mV
		79	-	121		-	V_{SENSE} = 100mV
		177	-	223		-	V_{SENSE} = 200mV
		470	-	530		-	V_{SENSE} = 500mV
Dynamic Characteristics							
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	µs	-	V_{SENSE} step 5mV to 500mV
		-	-	2.0		-	V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	µs	-	V_{SENSE} step 500mV to 0mV

Notes: 1. Referenced to GND
2. $V_{SENSE} = V_{IN} - V_{LOAD}$
Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

•G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

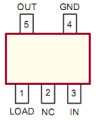
Note: Thermal testboard per JEDEC JESD51-7

Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} [1]	-0.5V to +450V
V_{OUT} [1]	-0.5V to +10V
V_{SENSE} [2]	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



5-Lead SOT-23
(top view)

Product Marking

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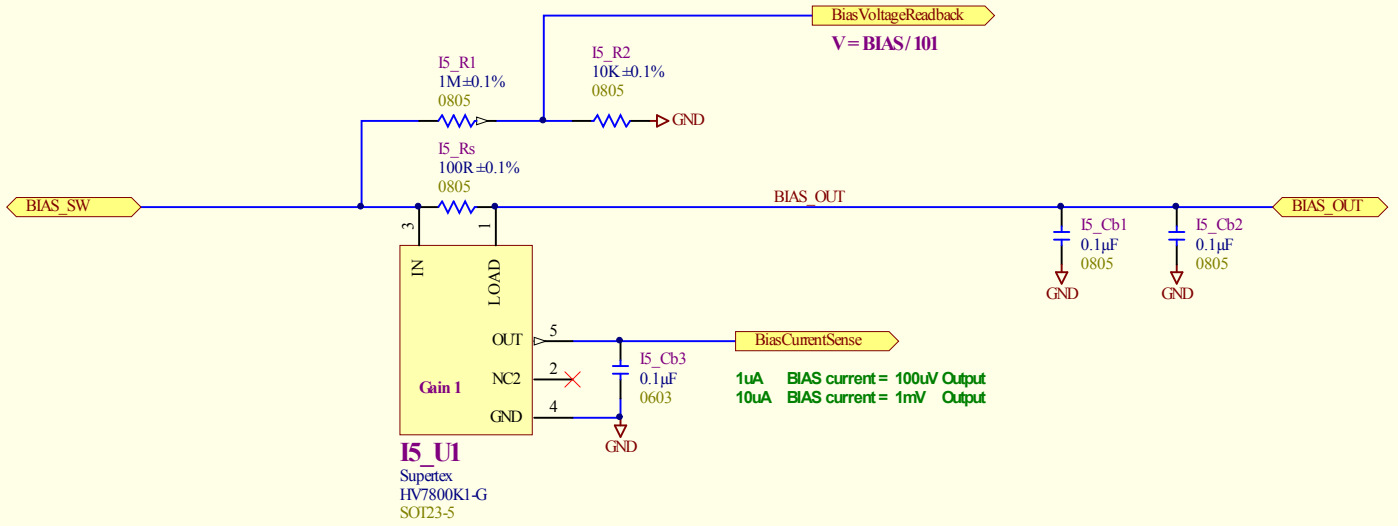
5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - BIAS Current Sense.SchDoc 5:10:23 PM



Electrical Characteristics (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units		Conditions
Supply							
V_{IN}	Supply voltage	8.0	-	450	V	*	---
I_Q	Quiescent supply current	-	-	50	µA	-	V_{IN} = 8V to 450V, V_{SENSE} = 0mV
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Notes: 1. Referenced to GND
2. $V_{SENSE} = V_{IN} - V_{LOAD}$
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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

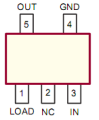
•G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



5-Lead SOT-23
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} [1]	-0.5V to +450V
V_{OUT} [1]	-0.5V to +10V
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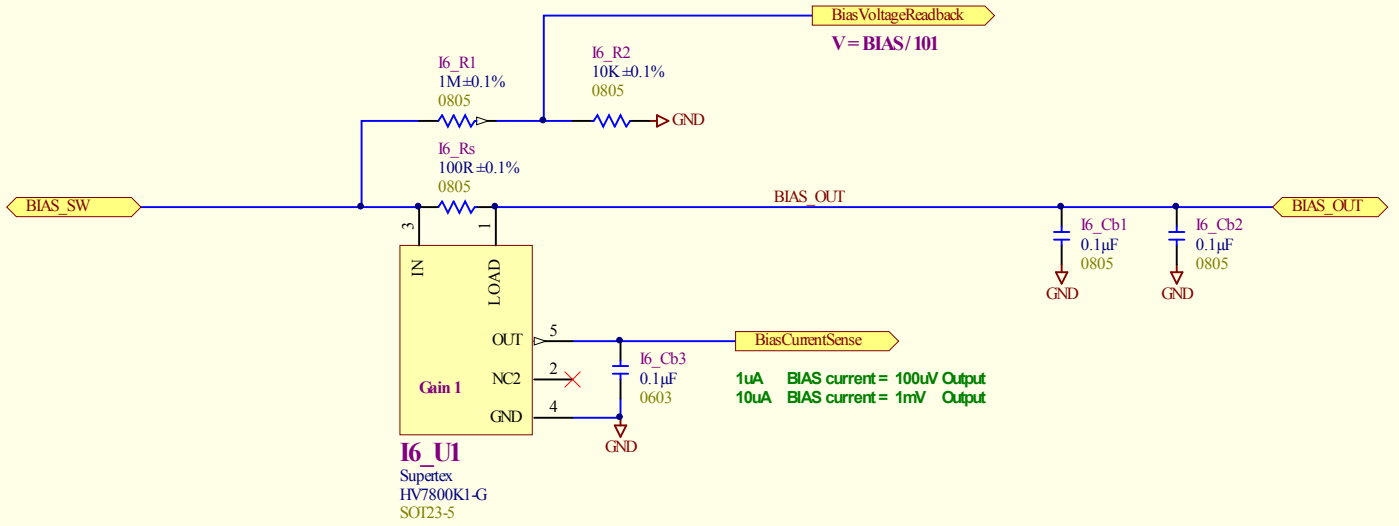
5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - BIAS Current Sense.SchDoc 5:10:23 PM



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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

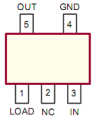
•G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



5-Lead SOT-23
(top view)

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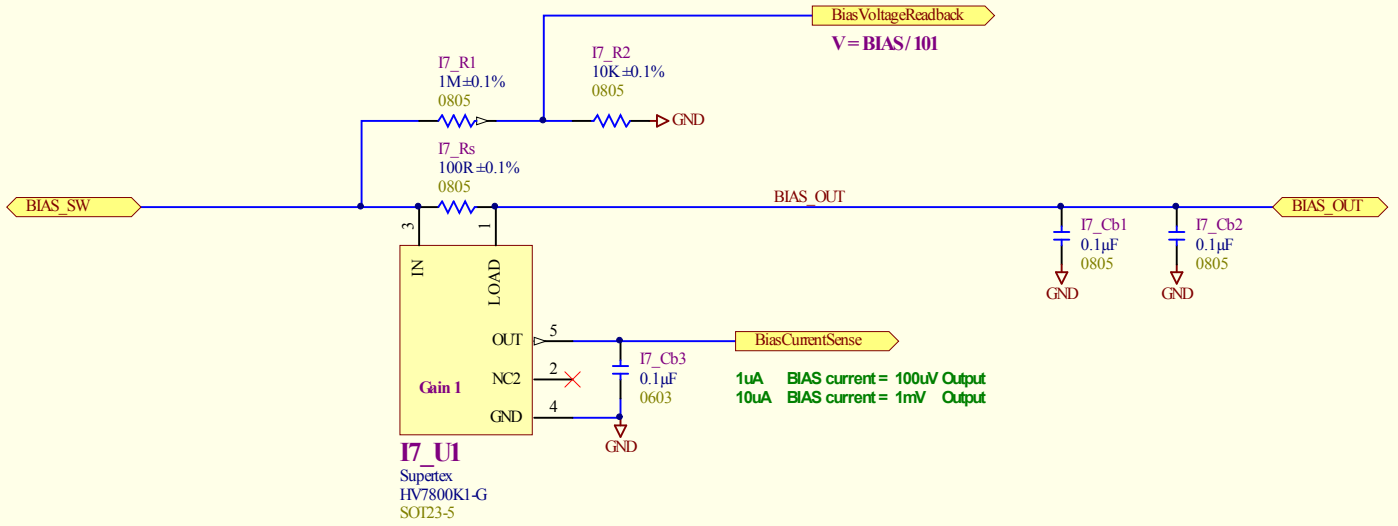
5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - BIAS Current Sense.SchDoc 5:10:23 PM



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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

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Thermal Resistance

Package	θ_{ja}
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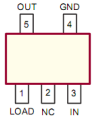
Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



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(top view)

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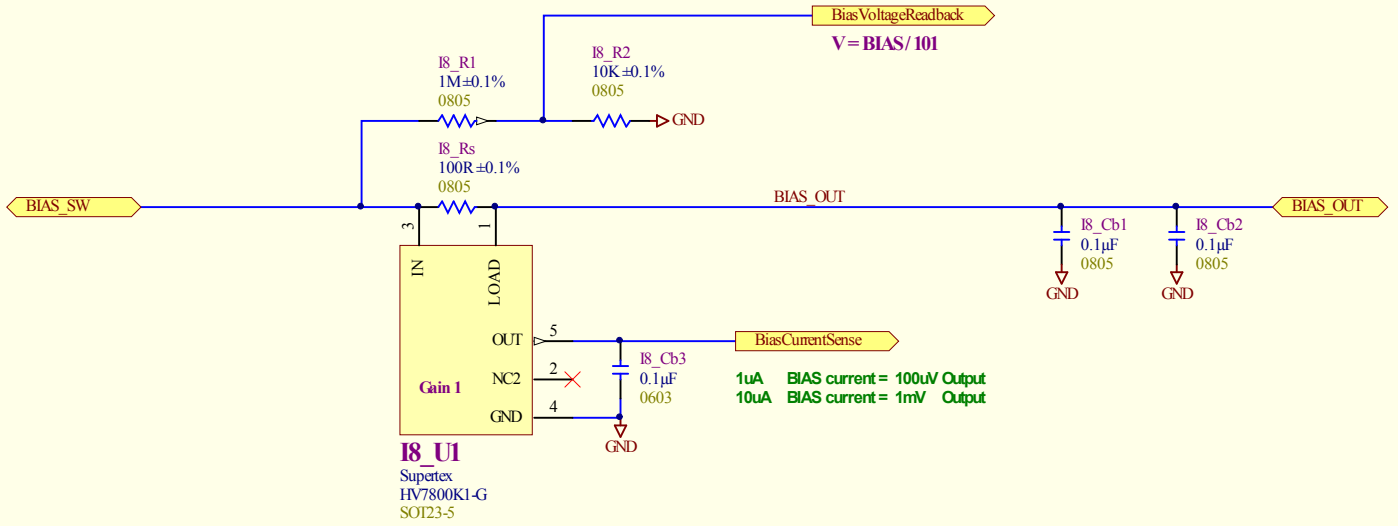
T2K FEB64 - BIAS Current Sense

Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - BIAS Current Sense.SchDoc 5:10:23 PM



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HV7800

Ordering Information

Device	Package Option
	5-Lead SOT-23
HV7800	HV7800K1-G

•G indicates package is RoHS compliant ('Green')

Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	191 °C/W

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Parameter	Value
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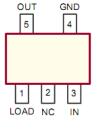
Pin Configuration



5-Lead SOT-23
(top view)

Product Marking

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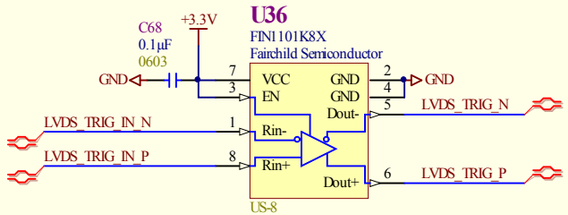
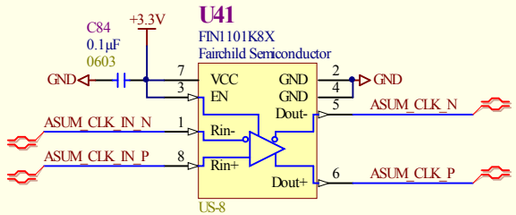
5-Lead SOT-23

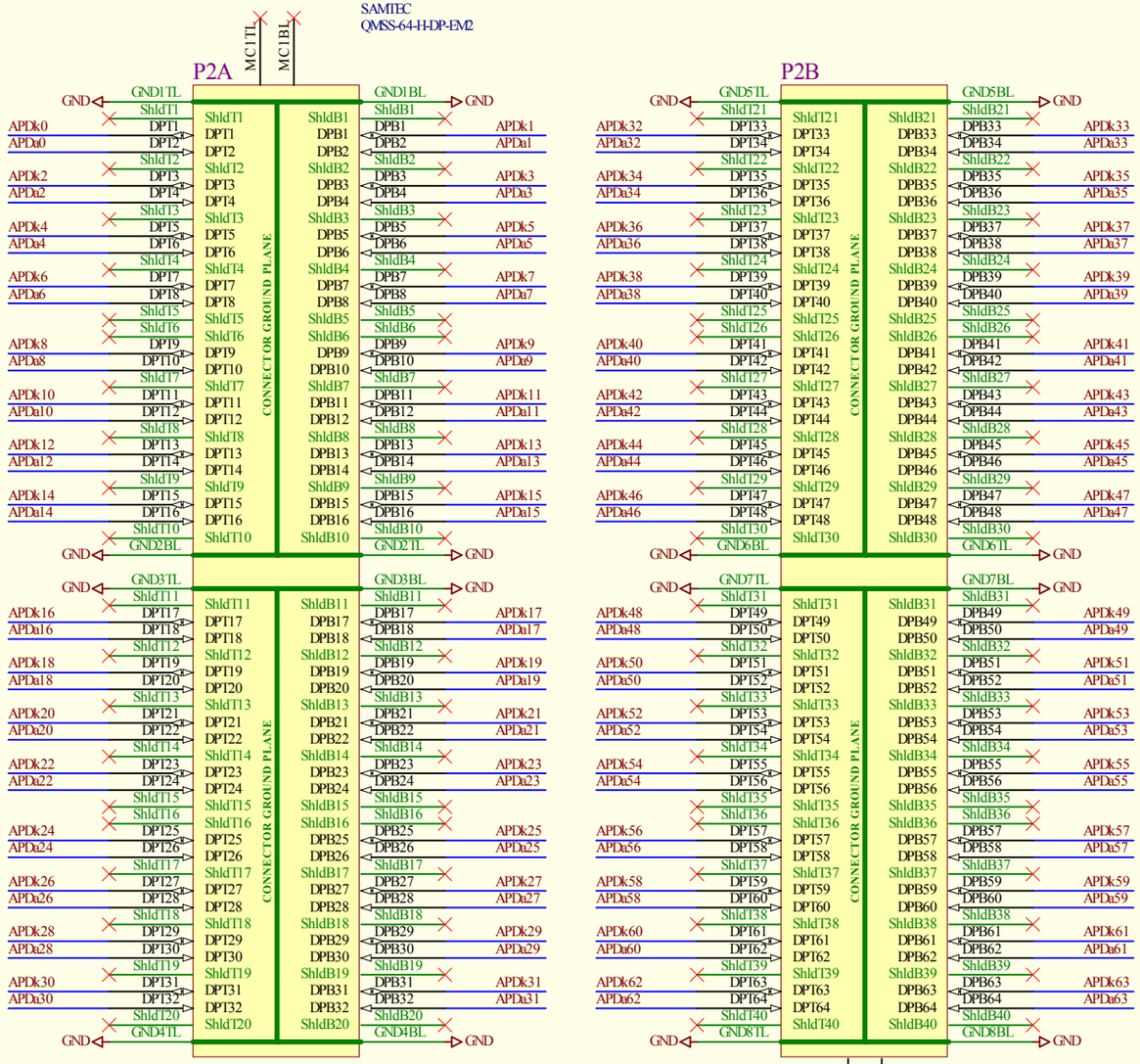
T2K FEB64 - BIAS Current Sense

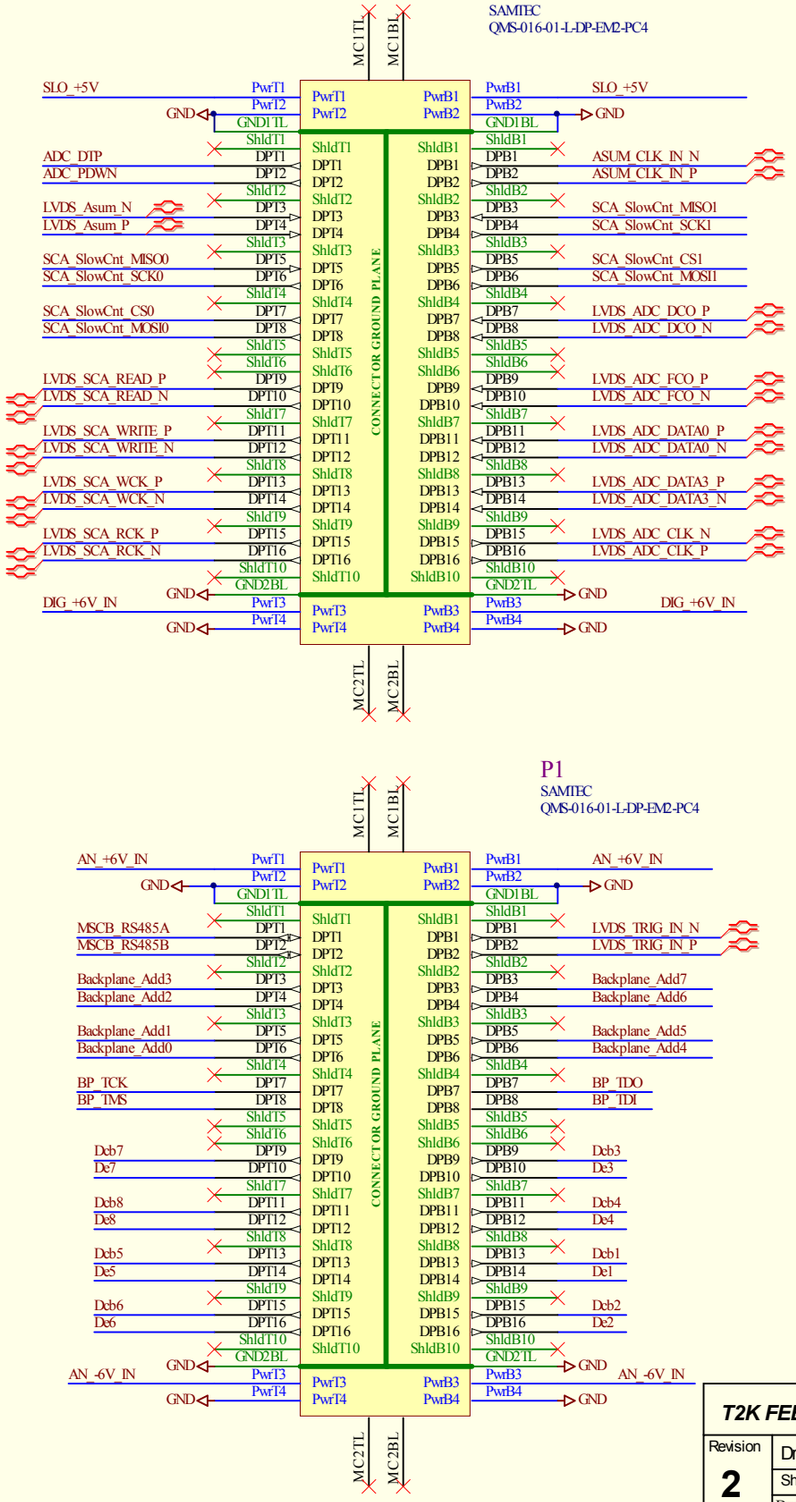
Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - BIAS Current Sense.SchDoc 5:10:23 PM









SCA Rd/Wrt Control

LVDS_SCA_WCK_P ↔ LVDS_SCA_WCK_P
LVDS_SCA_WCK_N ↔ LVDS_SCA_WCK_N
LVDS_SCA_RCK_P ↔ LVDS_SCA_RCK_P
LVDS_SCA_RCK_N ↔ LVDS_SCA_RCK_N
LVDS_SCA_READ_P ↔ LVDS_SCA_READ_P
LVDS_SCA_READ_N ↔ LVDS_SCA_READ_N
LVDS_SCA_WRITE_P ↔ LVDS_SCA_WRITE_P
LVDS_SCA_WRITE_N ↔ LVDS_SCA_WRITE_N

SCA Calibrate Trigger

LVDS_TRIG_P ↔ LVDS_TRIG_P
LVDS_TRIG_N ↔ LVDS_TRIG_N

ADC Control

LVDS_ADC_CLK_P ↔ LVDS_ADC_CLK_P
LVDS_ADC_CLK_N ↔ LVDS_ADC_CLK_N
LVDS_ADC_DCO_P ↔ LVDS_ADC_DCO_P
LVDS_ADC_DCO_N ↔ LVDS_ADC_DCO_N
LVDS_ADC_FCO_P ↔ LVDS_ADC_FCO_P
LVDS_ADC_FCO_N ↔ LVDS_ADC_FCO_N
LVDS_ADC_DATA0_P ↔ LVDS_ADC_DATA0_P
LVDS_ADC_DATA0_N ↔ LVDS_ADC_DATA0_N
LVDS_ADC_DATA3_P ↔ LVDS_ADC_DATA3_P
LVDS_ADC_DATA3_N ↔ LVDS_ADC_DATA3_N

SCA Slow Control

SCA_SlowCnt_MISO0 ↔ SCA_SlowCnt_MISO0
SCA_SlowCnt_MISO1 ↔ SCA_SlowCnt_MISO1
SCA_SlowCnt_SCK0 ↔ SCA_SlowCnt_SCK0
SCA_SlowCnt_SCK1 ↔ SCA_SlowCnt_SCK1
SCA_SlowCnt_MOSI0 ↔ SCA_SlowCnt_MOSI0
SCA_SlowCnt_MOSI1 ↔ SCA_SlowCnt_MOSI1
SCA_SlowCnt_CS0 ↔ SCA_SlowCnt_CS0
SCA_SlowCnt_CS1 ↔ SCA_SlowCnt_CS1

BP_TCK ↔ BP_TCK
BP_TMS ↔ BP_TMS
BP_TDO ↔ BP_TDO
BP_TDI ↔ BP_TDI

Backplane_Add[7..0] ↔ Backplane_Add[7..0]

Global LVDS Signals

ASUM_CLK_P ↔ ASUM_CLK_P
ASUM_CLK_N ↔ ASUM_CLK_N

ADC Control

ADC_DTP ↔ ADC_DTP
ADC_PDWN ↔ ADC_PDWN

LVDS Analog SUM Data

LVDS_Asum_P ↔ LVDS_Asum_P
LVDS_Asum_N ↔ LVDS_Asum_N

MSCB Slow Control

MSCB_RS485B ↔ MSCB_RS485B
MSCB_RS485A ↔ MSCB_RS485A

Temperature Sense Diodes

Dc[8..1] ↔ Dc[8..1]
Dcb[8..1] ↔ Dcb[8..1]

APD INPUTS

APDa[63..0] ↔ APDa[63..0]
APDk[63..0] ↔ APDk[63..0]

AN_+6V_IN ↔ AN_+6V_IN
AN_-6V_IN ↔ AN_-6V_IN

DIG_+6V_IN ↔ DIG_+6V_IN
SLO_+5V ↔ SLO_+5V

T2K FEB64 - Backplane Connections

Revision 2	Drawing #: 8		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 16	Size: B	
	Drawn by: Daryl Bishop	Date: 10/12/2008	

File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - Backplane Connections.SCHDOC 5:10:23 PM

ASUM_IN[7..0] ASUM_IN[7..0] ASUM_OUT[7..0] ASUM_OUT[7..0]

SUM1
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN0 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT0 / COMP_IN0

SUM2
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN1 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT1 / COMP_IN1

SUM3
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN2 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT2 / COMP_IN2

SUM4
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN3 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT3 / COMP_IN3

SUM5
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN4 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT4 / COMP_IN4

SUM6
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN5 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT5 / COMP_IN5

SUM7
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN6 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT6 / COMP_IN6

SUM8
T2K FEB_Rev2 - Analog SUM.SCHDOC
ASUM_IN7 — ASUM_IN — ASUM_OUT / COMP_IN — ASUM_OUT7 / COMP_IN7

U31
AD8564ARZ — 16-SOIC
R77 10R ±1% 0603 — C121 1.0µF 0603 — C123 0.1µF 0603 — +5V — GND
COMP_IN0 2 / THRESHOLD0 1 / ASUM_TRIG0 4
COMP_IN1 7 / THRESHOLD1 8 / ASUM_TRIG1 5
COMP_IN2 10 / THRESHOLD2 9 / ASUM_TRIG2 12
COMP_IN3 15 / THRESHOLD3 16 / ASUM_TRIG3 13
V+ Dig 11 — V+ ana 14 — V- ana 6 — GND 3
C126 0.1µF 0603 — C127 1.0µF 0603 — C130 0.1µF 0603 — C131 1.0µF 0603 — +5V — -5V — GND

16-Lead Narrow Body SO (S Suffix) R-16A
AD8564
–IN A / +IN A / GND / OUT A / OUT B / V–ANA / +IN B / –IN B
–IN D / +IN D / V+ANA / OUT D / OUT C / V+DIG / +IN C / –IN C

U30
AD8564ARZ — 16-SOIC
R76 10R ±1% 0603 — C120 1.0µF 0603 — C122 0.1µF 0603 — +5V — GND
COMP_IN4 2 / THRESHOLD4 1 / ASUM_TRIG4 4
COMP_IN5 7 / THRESHOLD5 8 / ASUM_TRIG5 5
COMP_IN6 10 / THRESHOLD6 9 / ASUM_TRIG6 12
COMP_IN7 15 / THRESHOLD7 16 / ASUM_TRIG7 13
V+ Dig 11 — V+ ana 14 — V- ana 6 — GND 3
C124 0.1µF 0603 — C125 1.0µF 0603 — C128 0.1µF 0603 — C129 1.0µF 0603 — +5V — -5V — GND

RP19 470R ±5% 0603 x 4 — CP17 0.1µF 0612
SUM_DAC0 THRESHOLD0 / SUM_DAC1 THRESHOLD1 / SUM_DAC2 THRESHOLD2 / SUM_DAC3 THRESHOLD3 — GND
SUM_DAC4 THRESHOLD4 / SUM_DAC5 THRESHOLD5 / SUM_DAC6 THRESHOLD6 / SUM_DAC7 THRESHOLD7 — GND
RP20 470R ±5% 0603 x 4 — CP18 0.1µF 0612

U37
Texas Instruments SN65LV1023AMDBREP
ASUM_DATA1 3 / ASUM_DATA2 4 / ASUM_DATA3 5 / ASUM_DATA4 6 / ASUM_DATA5 7 / ASUM_DATA6 8 / ASUM_DATA7 9 / ASUM_DATA8 10 / ASUM_CLK 14
Din0 Din1 Din2 Din3 Din4 Din5 Din6 Din7 Din8 Din9 TCLK
Do+ 22 LVDS_ASum_P → LVDS_ASum_P
Do- 21 LVDS_ASum_N → LVDS_ASum_N
DVcc 28 DVcc 27 — C3 10000pF 0603 — C4 0.1µF 0603 — +3.3V
DGND 16 DGND 15 — GND
AVcc 26 AVcc 17 AVcc 25 AGND 23 AGND 20 AGND 18 — C7 10000pF 0603 — C8 0.1µF 0603 — +3.3V — GND
ASUM_SYNC 1 → SYNC1 / SYNC2 2
ASUM_PdwnN 24 → PWRDN
DEN 19
TCLK/R/F 13
28-SSOP

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

U42
Texas Instruments TS5A3159ADBVR
R80 4K7 ±1% 0603 — +3.3V — GND
CPLD_POWER — SLO_+3.3V — C102 0.1µF 0603 — GND
IN 6 / V+ 5 / GND 2 / NOpen 1 / NClosed 3 / Common 4
CPLD_TDI 1 / XILINX_TDO 3 / XILINX_TDI 4
XILINX_TDO → XILINX_TDI < CPU TDO
SOT-23-6
CPLD Powered Down: XLINX_TDO = XILINX_TDI
CPLD Powered Up: CPLD_TDI = XILINX_TDI

U38B
XCR3064XL-10VQG44C — 44-VQFP
GND 42 43 44 — CPLD_TDI 1 / ASUM_DATA8 2 / ASUM_DATA7 3 / ASUM_DATA6 5 / ASUM_DATA5 6
I/O I/O I/O I/O, TDI I/O I/O I/O I/O — BANK 2

U38D
XCR3064XL-10VQG44C — 44-VQFP
JTAG_TMS — ASUM_DATA4 7 / ASUM_DATA3 8 / ASUM_DATA2 10 / ASUM_DATA1 11 / GND 12 13 14 15
I/O, TMS I/O I/O I/O I/O I/O I/O I/O — BANK 4

U38A
XCR3064XL-10VQG44C — 44-VQFP
ASUM_TRIG7 27 / ASUM_TRIG1 28 / ASUM_TRIG0 30 / ASUM_TRIG2 31 / XILINX_TDO 32 / ASUM_TRIG3 33 / GND 34 35
I/O I/O I/O I/O I/O, TDO I/O I/O I/O — BANK 1

U38C
XCR3064XL-10VQG44C — 44-VQFP
GND 18 19 20 21 — ASUM_TRIG4 22 / ASUM_TRIG5 23 / ASUM_TRIG6 25 / JTAG_TCK 26
I/O I/O I/O I/O I/O, TCK I/O I/O I/O — BANK 3

U32
Linear Technology LTC2600CGN#PBF 16-Bits — SSOP16
SUM_DAC_SCK 8 / SUM_DAC_DIN 9 / SUM_DAC_CSn 10 / SUM_DAC_CLRn 7 / 11
SCK Din Dout CS/LD CLR
Vout H 15 SUM_DAC7 / Vout G 14 SUM_DAC6 / Vout F 13 SUM_DAC5 / Vout E 12 SUM_DAC4 / Vout D 5 SUM_DAC3 / Vout C 4 SUM_DAC2 / Vout B 3 SUM_DAC1 / Vout A 2 SUM_DAC0
REF 6 ASUM_DAC_REF
VCC 16 — C142 0.1µF 0603 — C143 1.0µF 0603 — +5V
GND 1 — GND

Pin Compatible Versions
LTC2610: 14Bits
LTC2620: 12Bits
LTC1660: 10Bits
LTC1665: 8-Bits

ORDER PART NUMBER
LTC2600CGN
LTC2600IGN
LTC2610CGN
LTC2610IGN
LTC2620CGN
LTC2620IGN
GN PART MARKING
2600
2600I
2610
2610I
2620
2620I

TOP VIEW — GN PACKAGE 16-LEAD PLASTIC SSOP — T_{JMAX} = 125°C, θ_{JA} = 150°C/W

U39
Texas Instruments SN65LVDS2DBVR — SOT23-5
C167 0.1µF 0603 — +3.3V — GND
ASUM_CLK_P — ASUM_CLK_N — RT6 100R 1% 0603
3 / 4 — Vcc 1 / R2 / Gnd 2 — 5 — GND

VREF2
Analog Devices Inc REF198FSZ 4.096 V ±0.12% 10 ppm/°C — 8-SOIC
NC 8 / NC 7 / OUT 6 / NC_TP5 5 / NC_TP1 1 / VCC 2 / SLEEP 3 / GND 4
C141 1.0µF 0603 — GND
C138 0.1µF 0603 — +5V — GND

ASUM_TESTin — ASUM_CLK 40 / ASUM_TESTin 39 / 38 / GND 37 / +3.3V 4
IN0/CLK0 IN1/CLK1 IN2/CLK2 IN3/CLK3 PORT_EN
44-VQFP

U38E
XCR3064XL-10VQG44C — 44-VQFP

U38F
XCR3064XL-10VQG44C — 44-VQFP
+3.3V — VCC 41 VCC 29 — VCC 9 VCC 17 — +3.3V
C165 0.1µF 0603 — C166 0.1µF 0603 — C163 0.1µF 0603 — C164 0.1µF 0603

U38G
XCR3064XL-10VQG44C — 44-VQFP
GND 36 GND 24 — GND 16 — GND

DB Package SN65LV1023A Serializer

T2K FEB64 - APD SUM x 8

Revision	Drawing #: 9		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
2	Sheet #: 9 of 16	Size: B	
	Drawn by: D.Bishop	Date: 10/12/2008	
File: G:\AHW\T2K\T2K_FEB64\Rev2\T2K FEB_Rev2 - APD SUM.SCHDOC			5:10:23 PM