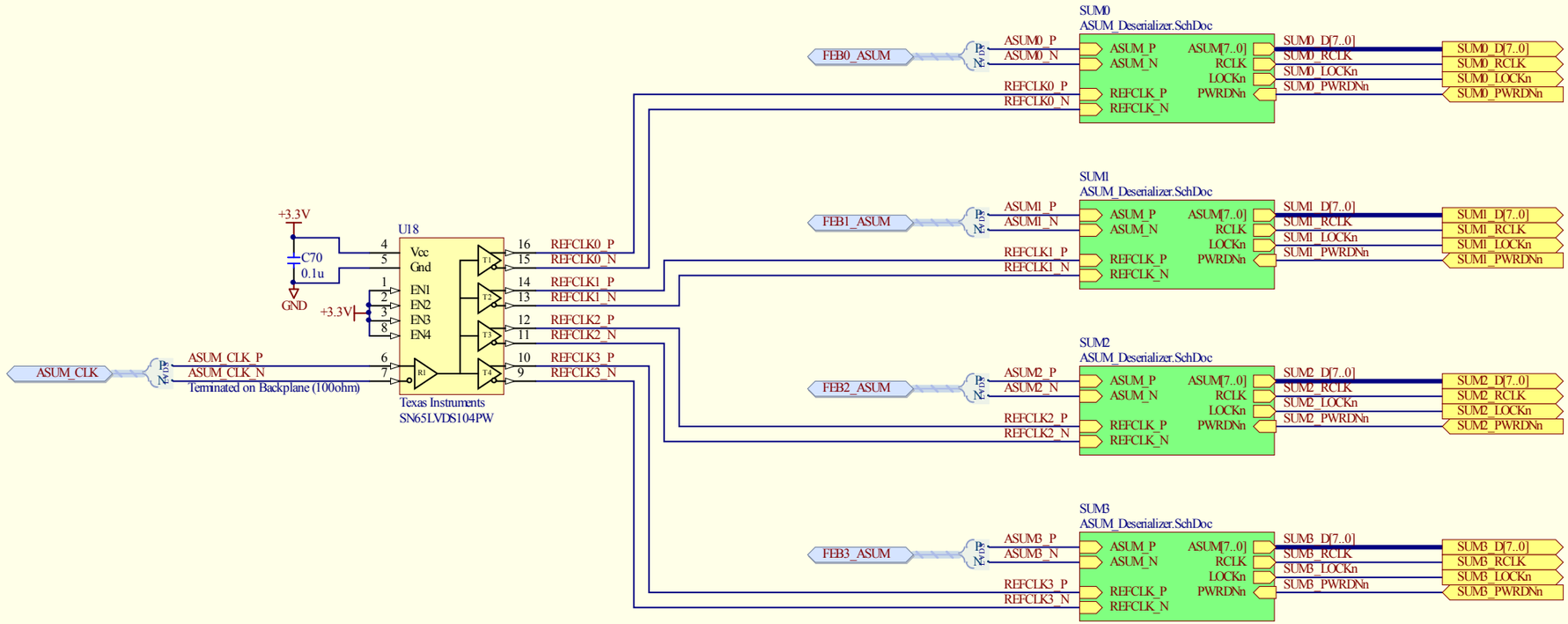
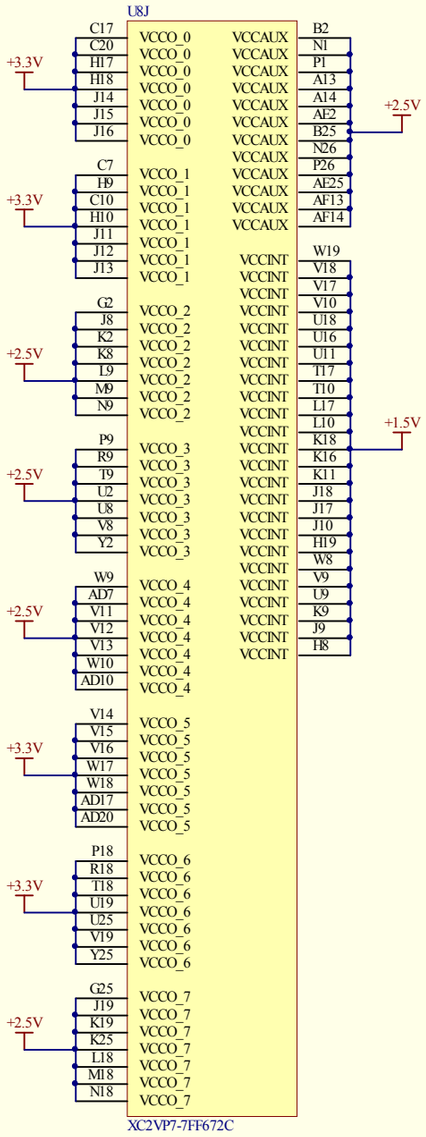


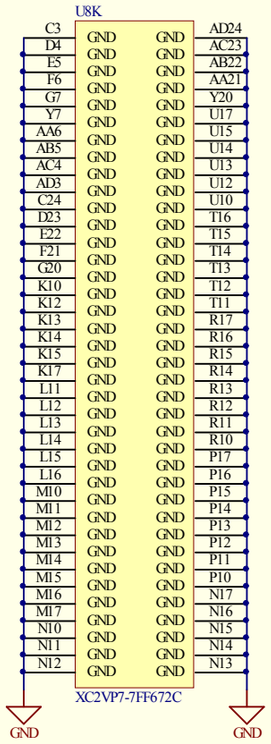
T2K_CMB - Crate Master Board (ASUM)

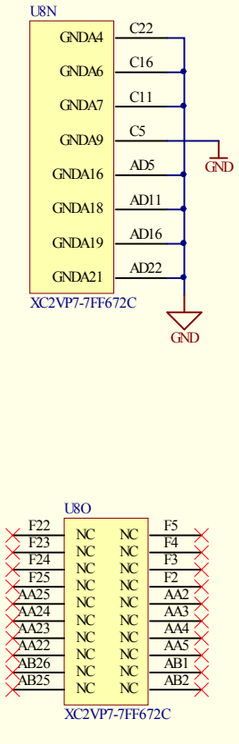
Revision **B**	Drawing #: 2		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 2 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\AnalogSUM.SchDoc			12:19:33 PM

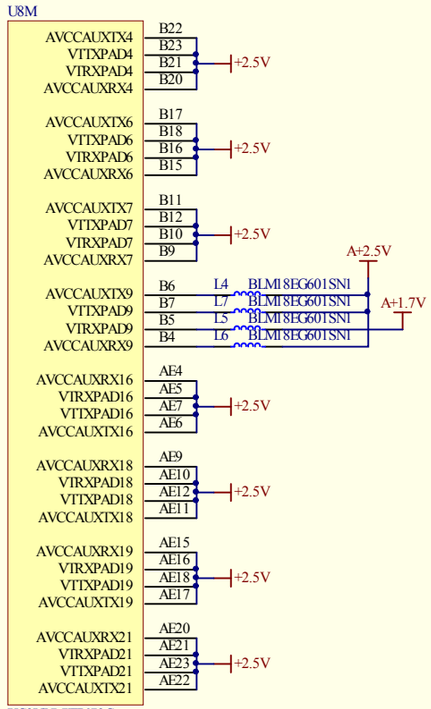
FPGA POWER PINS

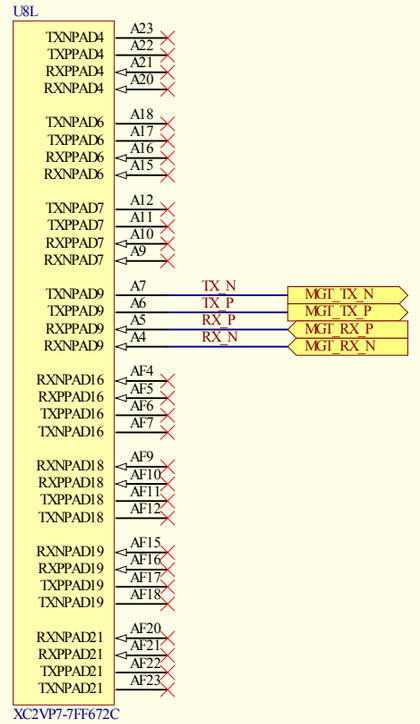


FPGA GROUND PINS

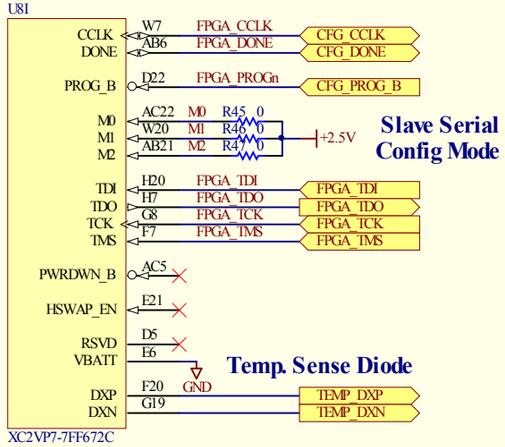




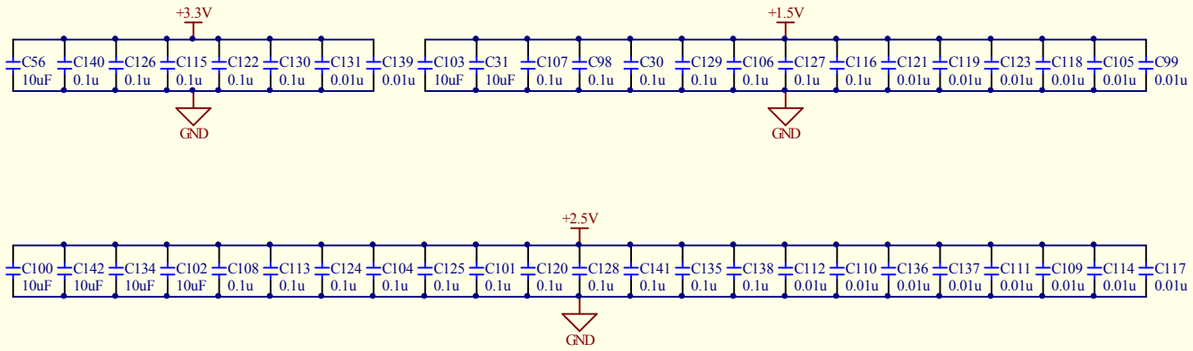




FPGA CONFIG PINS



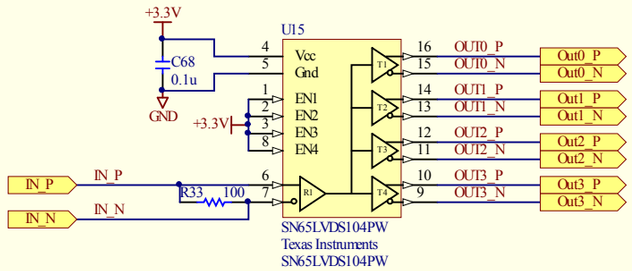
FPGA BYPASS CAPS



Revision	B
Drawing #:	9
Sheet #:	9 of 14
Size:	B
Drawn by:	C. Ohlmann
Date:	18/12/2008
File:	M\edevel\Altium\Projects\T2K_CMB_RevB\FPGA_PowerConfigRocketIO.SchDoc
	12:19:33 PM

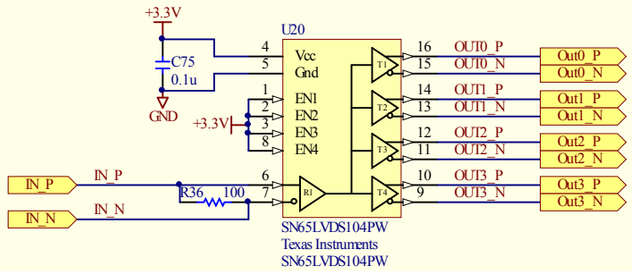
T2K_CMB - Crate Master Board (FPGA - Power and Config)

TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3



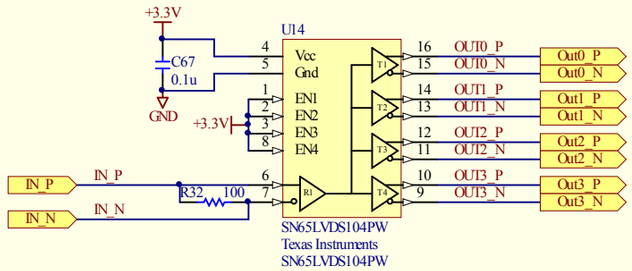
T2K_CMB - Crate Master Board (1:4 LVDS Fanout)

Revision B	Drawing #: 8		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\LVDSFanout1to4.SchDoc			12:19:33 PM



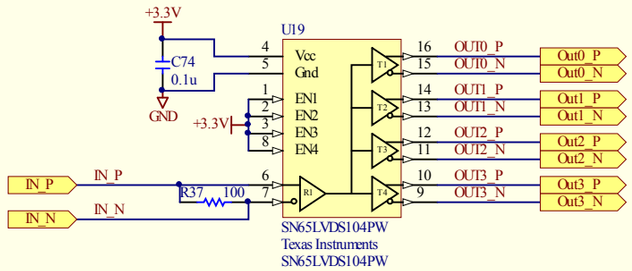
T2K_CMB - Crate Master Board (1:4 LVDS Fanout)

Revision B	Drawing #: 8		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\LVDSFanout1to4.SchDoc			12:19:33 PM



T2K_CMB - Crate Master Board (1:4 LVDS Fanout)

Revision B	Drawing #: 8		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\LVDSFanout1to4.SchDoc			12:19:33 PM



T2K_CMB - Crate Master Board (1:4 LVDS Fanout)

Revision **B**	Drawing #: 8		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
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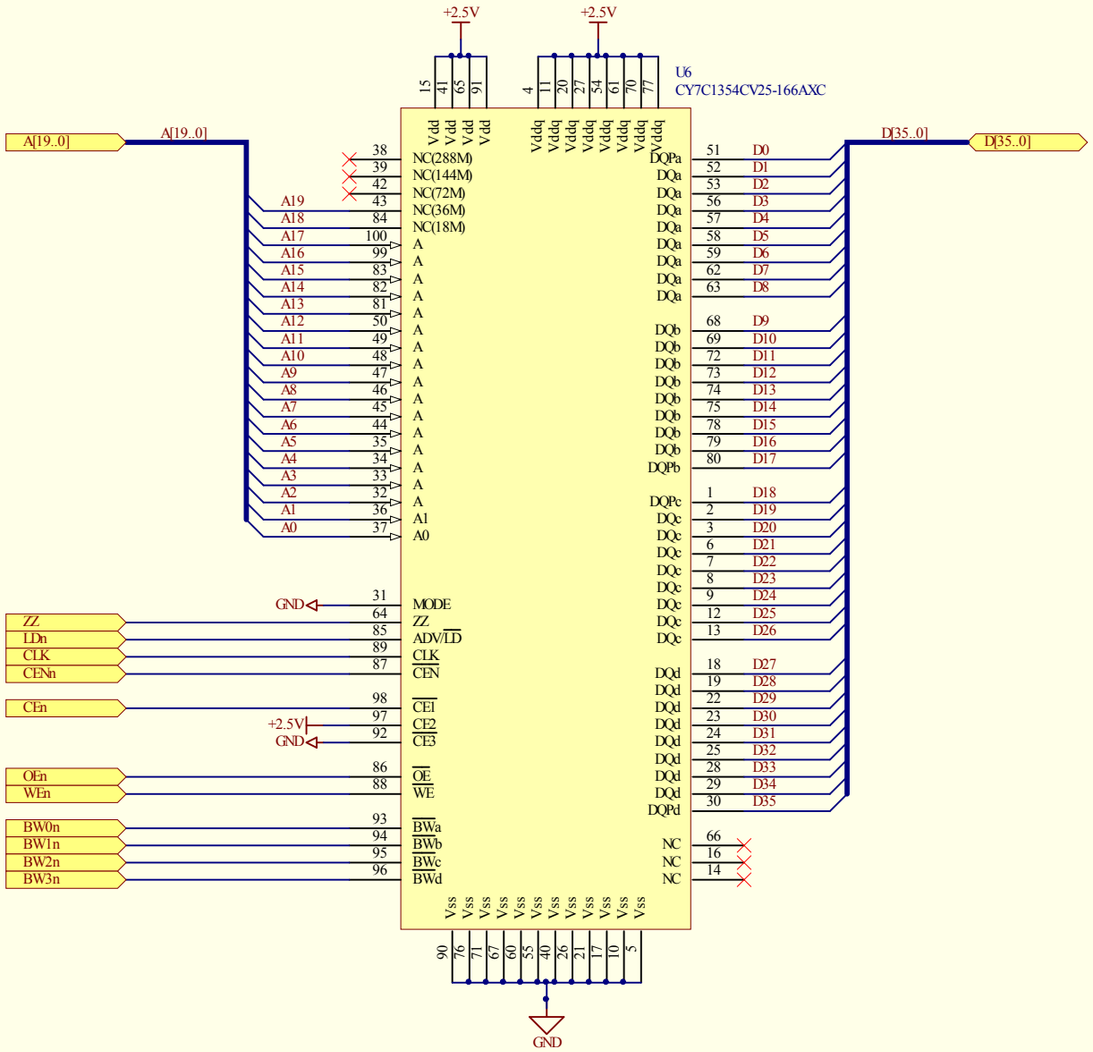
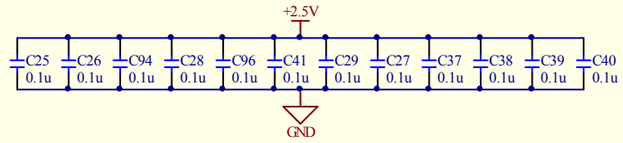
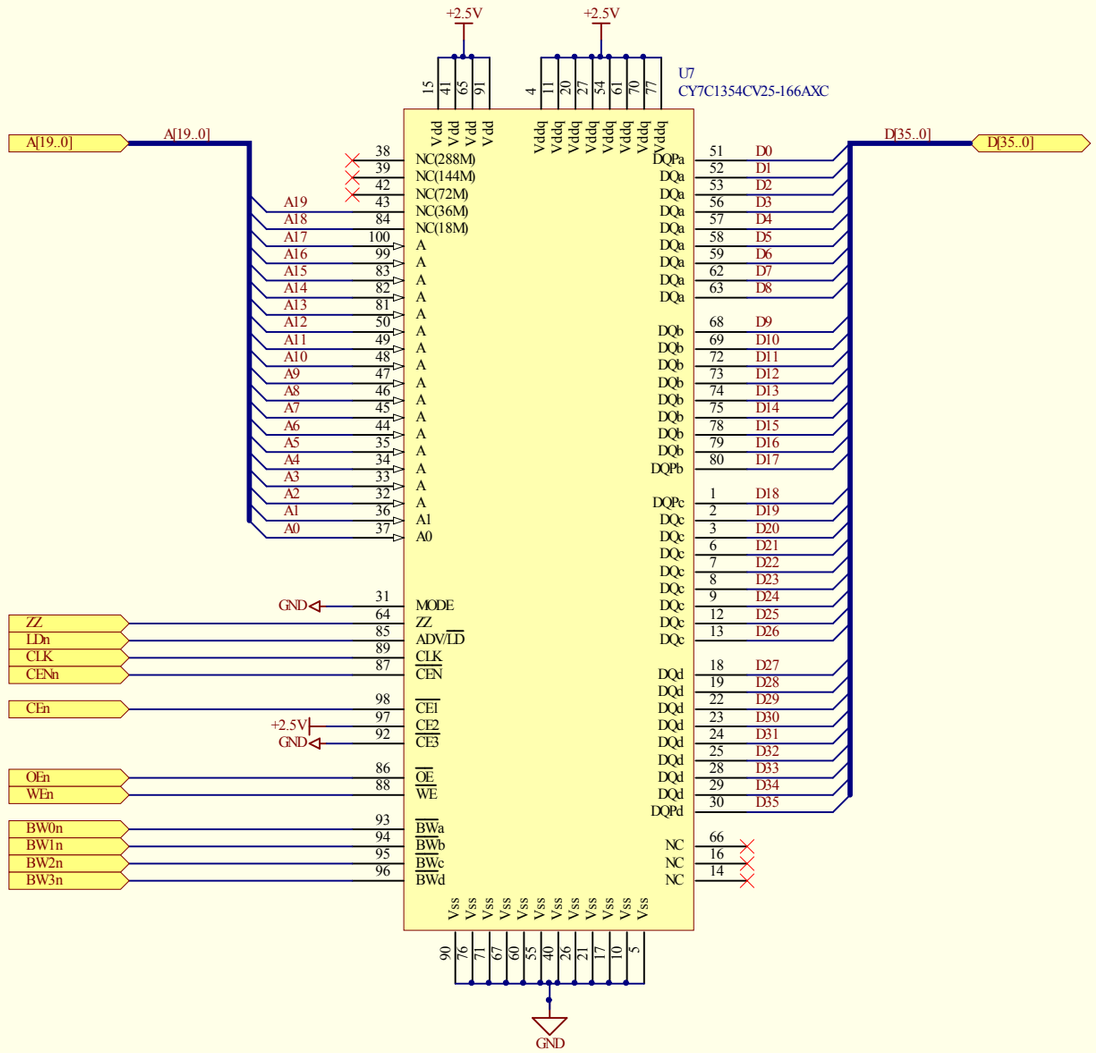
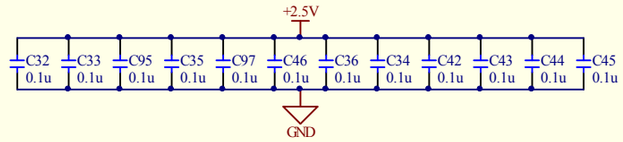




T2K_CMB - Crate Master Board (SRAM)

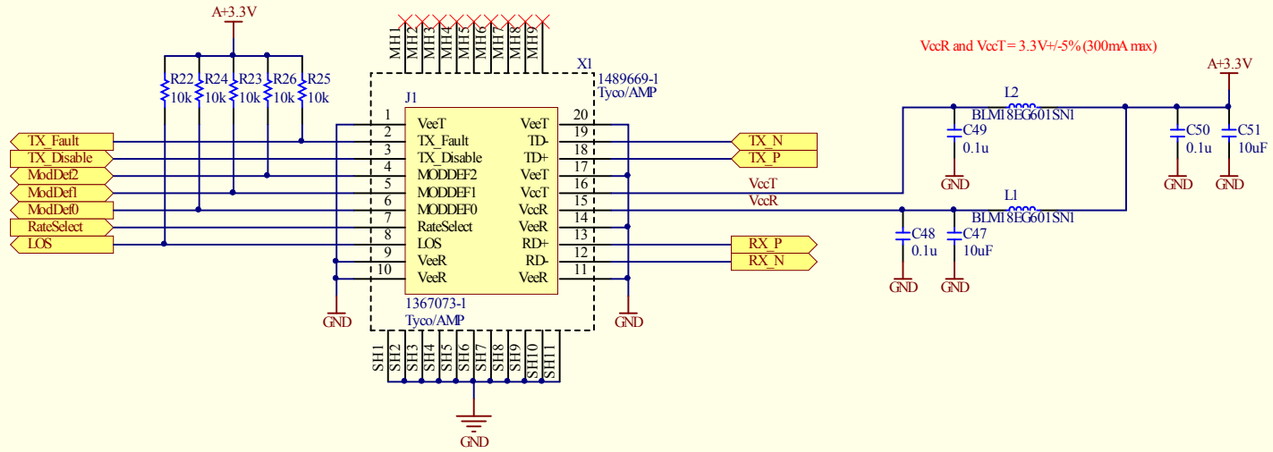
Revision B	Drawing #: 10		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 10 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\MemorySRAM.SchDoc			12:19:34 PM





T2K_CMB - Crate Master Board (SRAM)

Revision B	Drawing #: 10		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 10 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M\edevel\Altium\Projects\T2K_CMB_RevB\MemorySRAM.SchDoc			12:19:34 PM



T2K_CMB - Crate Master Board (Optical Link)

Revision B	Drawing #: 11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 11 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\OpticalLink.SchDoc			12:19:34 PM

SC3.3V
C17 0.1u
C16 0.1u
C10 0.1u
C93 0.1u
GND

CPU_TCK
CPU_TMS
CPU_TDI
R49 4.7K
SC3.3V
CPU_TDO
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TDO

U5
SC3.3V
C92 0.1u
GND
VCC
485_RXD
485_TX_EN
485_TXD
MSCB_RS485B
MSCB_RS485A
GND
MAX3483ECSA+

+3.3V
R11 2K
+3.3V_Mon
R10 4.7K
GND

+2.5V
R12 2K
+2.5V_Mon
R13 4.7K
GND

A+3.3V
R17 2K
A+3.3V_Mon
R15 4.7K
GND

A+2.5V
R16 2K
A+2.5V_Mon
R14 4.7K
GND

SC3.3V
R19 4.7K
0.7V
SST_REF
R18 2K
C13 0.1u
GND

SC3.3V
L3 BLM18EG601SN1
C14 0.1u
GND
C11 0.1u
C91 4.7u
GND
Vref_2.4V
Is_+4V
+4Vsupply
A+3.3V_Mon
A+2.5V_Mon
+1.5V
+1.8V
+2.5V_Mon
+3.3V_Mon
SST_IO

U3
C8051F133-GQ
Silicon Laboratories
C8051F131
C8051F133
TQFP-64
CP1-
CP1+
CP0-
CP0+
AGND
AV+
Vref
Vref0
AIN0.0
AIN0.1
AIN0.2
AIN0.3
AIN0.4
AIN0.5
AIN0.6
AIN0.7
P0.7
P3.0
P3.1
P3.2
P3.3
P3.4
P3.5
VDD
DGND
P3.6
P3.7
P2.0
P2.1
P2.2
P2.3
P2.4
CLK_SEL
CRATE_A0
CRATE_A1
CRATE_A2
CRATE_A3
CRATE_A4
CRATE_A5
SC3.3V
GND
CFG_RECOVER
WATCHDOG
+4V_ENn
+4V_OCn
XTAL1
XTAL2
MONEN
P1.7/AIN2.7
P1.6/AIN2.6
P1.5/AIN2.5
P1.4/AIN2.4
VDD
GND
P1.3/AIN2.3
P1.2/AIN2.2
P1.1/AIN2.1
P1.0/AIN2.0
P2.7
P2.6
P2.5
SC3.3V
R7 4.7K
ROM_CSn
SPI_MISO
ROM_WPn
SC3.3V
GND
ROM_HOLDn
SPI_SCK
SPI_MOSI
SST_DRV
SC_DEBUG2
SC_DEBUG1
SC_DEBUG0
SC_TX_EN
485_TXD
485_RXD

CLK_SEL
Source Clock Select
- Open Drain Output
- 0 = Onboard Oscillator
- 1 = RJ45 Clock

CLK_SEL
CRATE_A[5..0]
WATCHDOG
CFG_RECOVER
+4V_ENn
+4V_OCn
SC_DEBUG[2..0]

Imon_+4V
R2 2K
Is_+4V
R1 4.7K
GND

+4V_IN
R5 4.7K
+4Vsupply
R4 4.7K
GND

U30
SC3.3V
SPI_MOSI
SPI_MISO
SPI_SCK
ROM_CSn
ROM_HOLDn
ROM_WPn
SI
SO
SCK
CS
HOLD
WP
VCC
GND
C154 0.1u
GND
AT25160AN-10SU-2.7
Atmel

Temperature Sensor

SST_DRV
R8 10K
SST_IO
R9 10K
GND
SC3.3V
GND
C7 0.1u
GND
U4
ADD = 0x48
SST
ADD0
ADD1
RSVD
VCC
GND
D1+
D1-
D2+
D2-
ADT7486A
TEMP_D1+
TEMP_D1-
Q1
MMBT3904

T2K_CMB - Crate Master Board (Slow Control)

Revision	Drawing #: 12		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
B	Sheet #: 12 of 14	Size: B		
	Drawn by: C. Ohlmann	Date: 18/12/2008		
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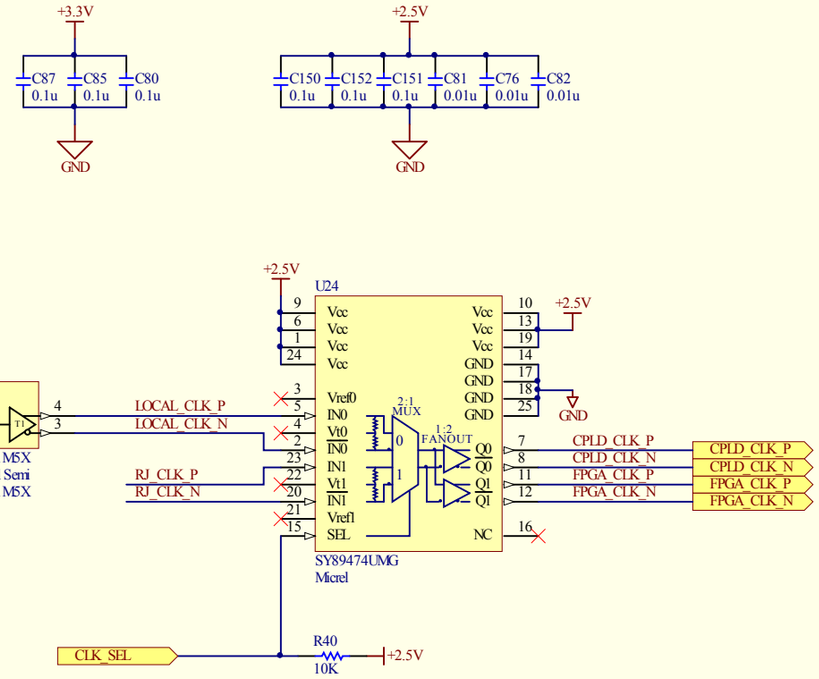
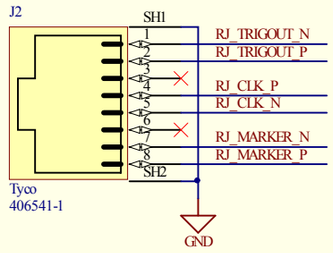
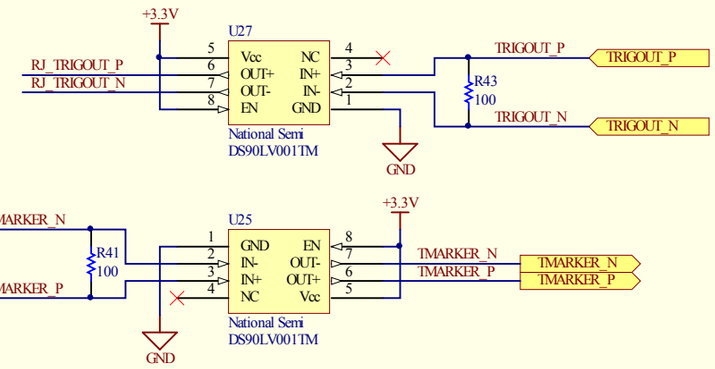


Cable Termination (Standard)

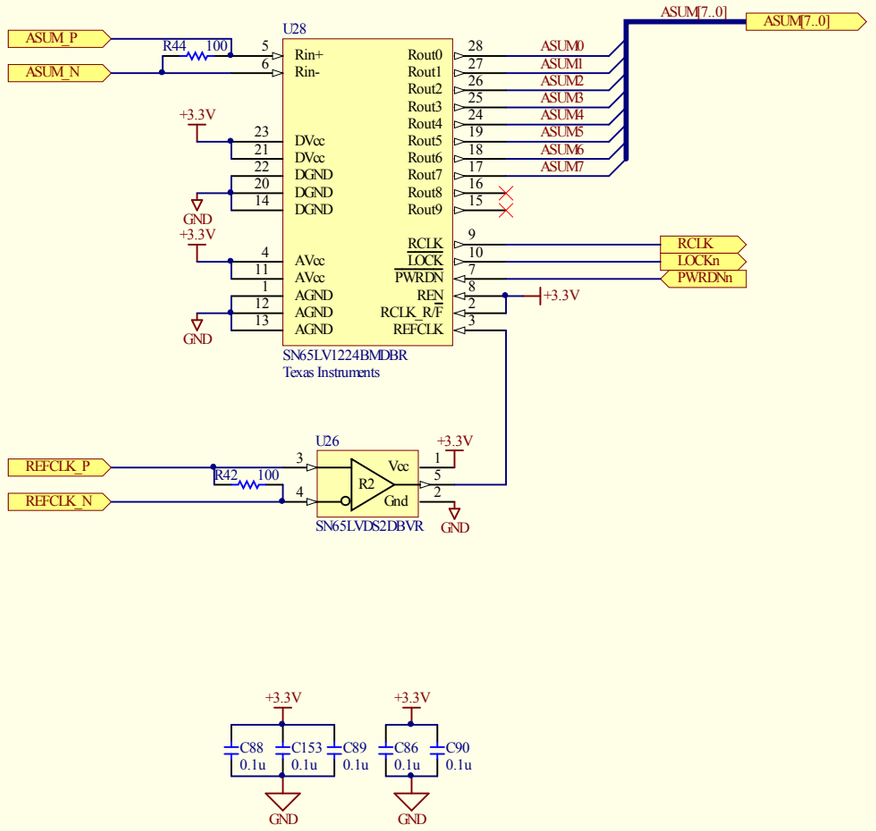
WHITE/orange
ORANGE/white
WHITE/green
BLUE/white
WHITE/blue
GREEN/white
WHITE/brown
BROWN/white





T2K_CMB - Crate Master Board (Clock / Trigger)

Revision **B**	Drawing #: 13		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 13 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M\edevel\Altium\Projects\T2K_CMB_RevB\TimingMarkerAndTrigger.SchDoc			12:19:34 PM



T2K_CMB - Crate Master Board (ASUM Deserializer)

Revision B	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 3 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\ASUM_Deserializer.SchDoc			12:19:34 PM

BackplaneConnections
BackplaneConnections.SchDoc

TMARKER_P
TMARKER_N
LPB_Signals
FEB0_Signals
FEB1_Signals
FEB2_Signals
FEB3_Signals
ASUM_CLK
CRATE_A[5..0]
MSCB_A
MSCB_B
SC5V_IN
+4V_IN
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO

TMARKER_P
TMARKER_N
LPB
FEB0
FEB1
FEB2
FEB3
ASUM_CLK
CRATE_A[5..0]
MSCB_A
MSCB_B

FPGA1
FPGA_PowerConfigRocketIO.SchDoc;FPGA_IOBank0-3.SchDoc;FPGA_IOBank4-7.SchDoc

LPB_Signals
FEB0_Signals
FEB1_Signals
FEB2_Signals
FEB3_Signals
ASUM_CLK
CRATE_A[5..0]
TEMP_DXP
TEMP_DXN
SC_DEBUG[2..0]
CLK_SEL
JTAG_TCK
JTAG_TMS
CPLD_TDO
FPGA_TDI
FPGA_TDO
TRIGOUT_P
TRIGOUT_N
FPGA_CLK_P
FPGA_CLK_N

ASUM
AnalogSUM.SchDoc

ASUM_CLK
FEB0.ASUM
FEB1.ASUM
FEB2.ASUM
FEB3.ASUM
FEB0_ASUM
FEB1_ASUM
FEB2_ASUM
FEB3_ASUM
SUM0_D[7..0]
SUM0_RCLK
SUM0_LOCKn
SUM0_PWRDNn
SUM1_D[7..0]
SUM1_RCLK
SUM1_LOCKn
SUM1_PWRDNn
SUM2_D[7..0]
SUM2_RCLK
SUM2_LOCKn
SUM2_PWRDNn
SUM3_D[7..0]
SUM3_RCLK
SUM3_LOCKn
SUM3_PWRDNn

SlowControl
SlowControl.SchDoc

MSCB_RS485A
MSCB_RS485B
TEMP_D1+
TEMP_D1-
CRATE_A[5..0]
CLK_SEL
+4V_ENn
+4V_OCn
Imon_+4V
+4V_IN
SC_DEBUG[2..0]
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TDO
WATCHDOG
CFG_RECOVER

VoltageRegulators
VoltageRegulators.SchDoc

SC5V_IN
+4V_IN
+4V_ENn
+4V_OCn
Imon_+4V

Configuration
CPLDandFlashMemory.SchDoc

CPLD_TCK
CPLD_TMS
CPLD_TDI
CPLD_TDO
CFG_RECOVER
WATCHDOG
FAIL_MODE[1..0]
CFG_RELOAD
FPGA_INITn
FPGA_DONE
FPGA_PROGn
FPGA_CCLK
FPGA_D0/DIN
FLASH_A[21..0]
FLASH_D[15..0]
FLASH_STS
FLASH_CEn
FLASH_OEn
FLASH_WEn
FLASH_VPEN
FLASH_RPn
FLASH_BYTEn
CPLD_CLK_P
CPLD_CLK_N

RECOVER
WATCHDOG

TimingMarkerAndTrigger
TimingMarkerAndTrigger.SchDoc

TMARKER_P
TMARKER_N
TRIGOUT_P
TRIGOUT_N
FPGA_CLK_P
FPGA_CLK_N
CPLD_CLK_P
CPLD_CLK_N
CLK_SEL

SRAM1
MemorySRAM.SchDoc

M1_A[19..0]
M1_D[35..0]
M1_ZZ
M1_CLK
M1_LDn
M1_CEn
M1_CENn
M1_OEn
M1_WEn
M1_BW0n
M1_BW1n
M1_BW2n
M1_BW3n

SRAM2
MemorySRAM.SchDoc

M2_A[19..0]
M2_D[35..0]
M2_ZZ
M2_CLK
M2_LDn
M2_CEn
M2_CENn
M2_OEn
M2_WEn
M2_BW0n
M2_BW1n
M2_BW2n
M2_BW3n

OpticalLink
OpticalLink.SchDoc

ModDef0
ModDef1
ModDef2
RateSelect
LOS
TX_Fault
TX_Disable
MGT_TX_P
MGT_TX_N
MGT_RX_P
MGT_RX_N

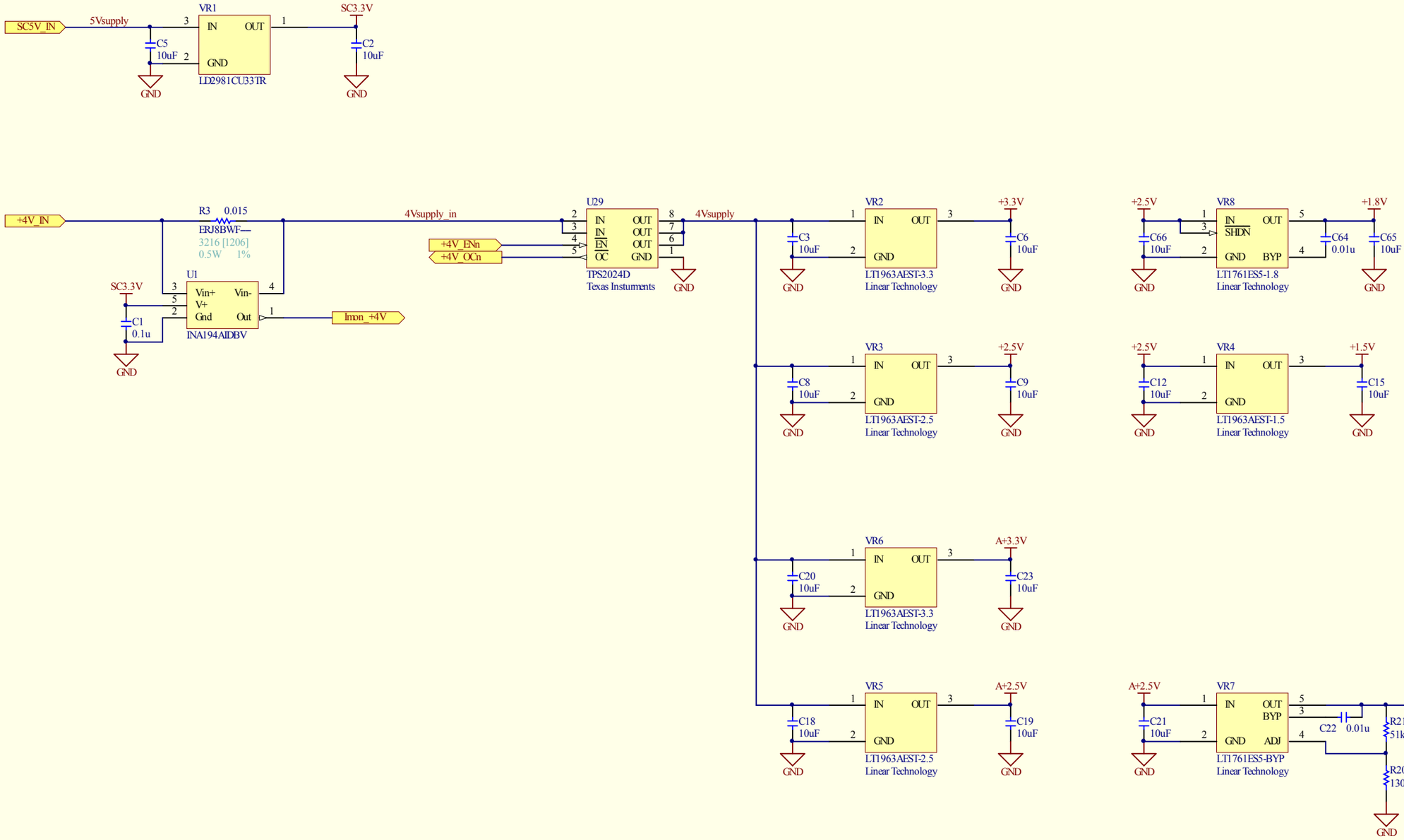
JTAG pinout compatible with Silicon Technologies USB DEBUG ADAPTER

+3.3V
P3
GND
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
TSW-105-08-S-D-RA
Samtec

SC3.3V
+3.3V
U2
IN
V+
GND
NO
COM
NC
FPGA_TDO
CPU_TDI
JTAG_TDI
C155
0.1u
TS5A3159ADBVR

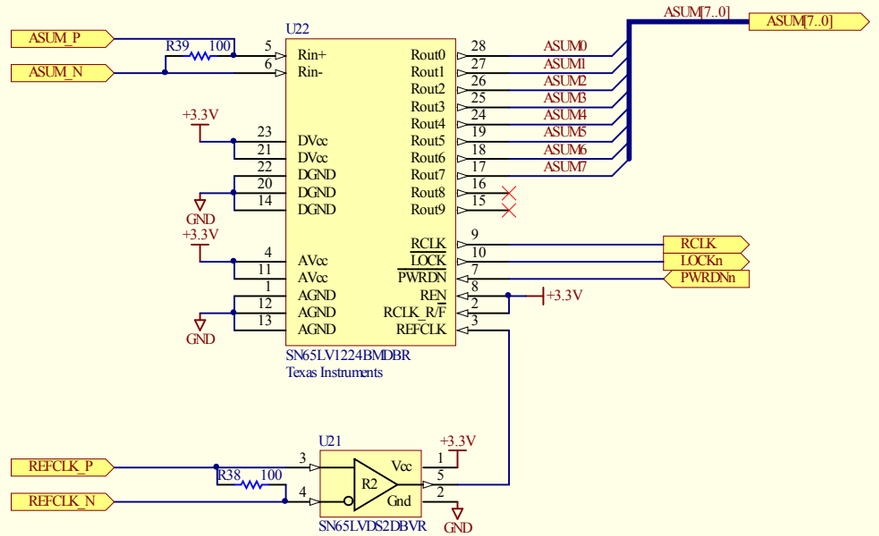
T2K_CMB - Crate Master Board

Revision B	Drawing #: 1		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 1 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\TopLevel.SchDoc			12:19:34 PM



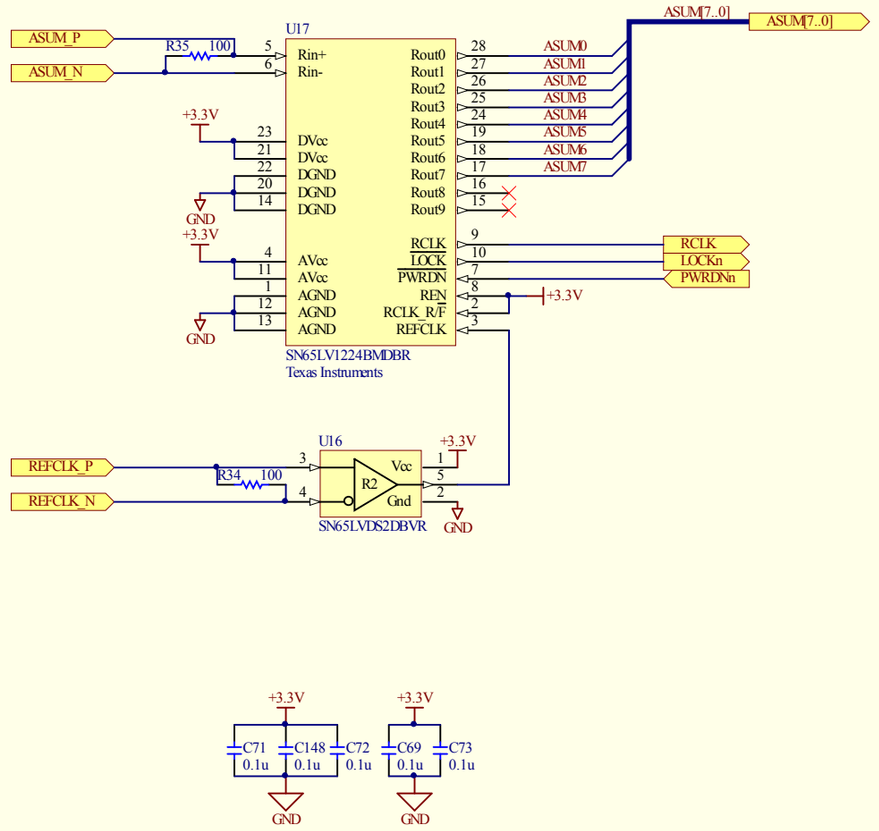
T2K_CMB - Crate Master Board (Voltage Regulators)

Revision B	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\VoltageRegulators.SchDoc			12:19:34 PM



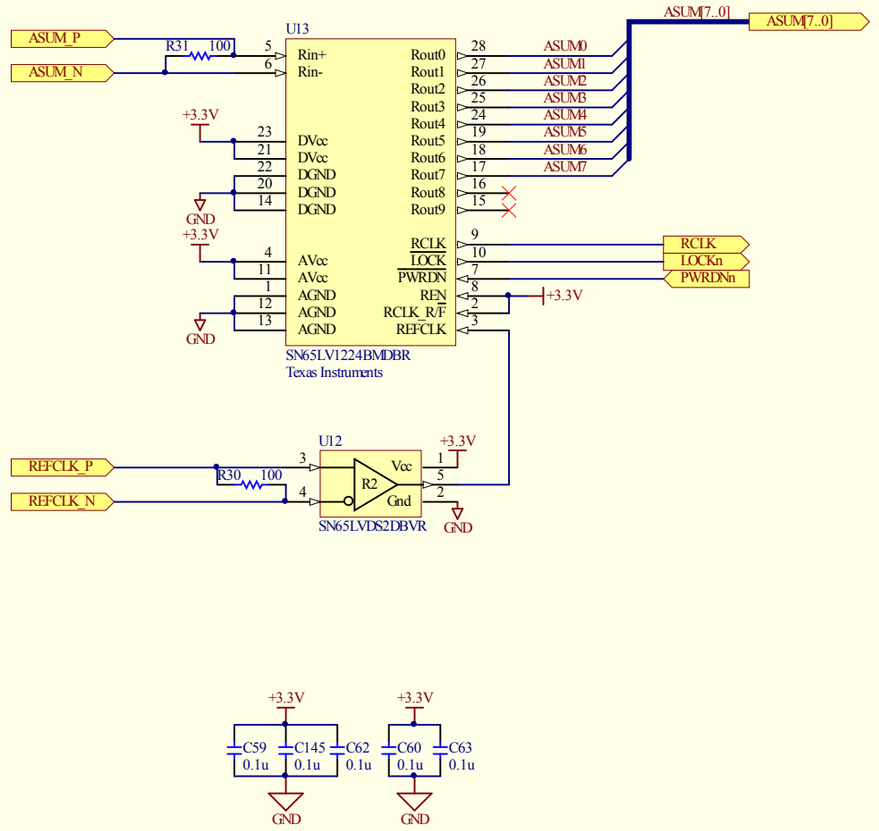
T2K_CMB - Crate Master Board (ASUM Deserializer)

Revision B	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 3 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\ASUM_Deserializer.SchDoc			12:19:34 PM



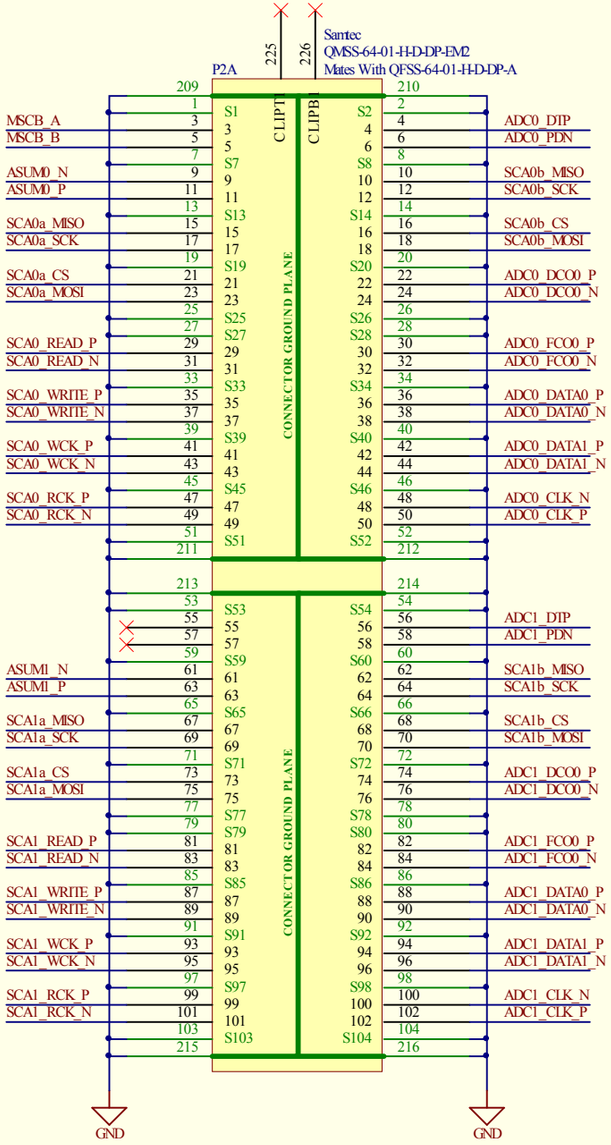
T2K_CMB - Crate Master Board (ASUM Deserializer)

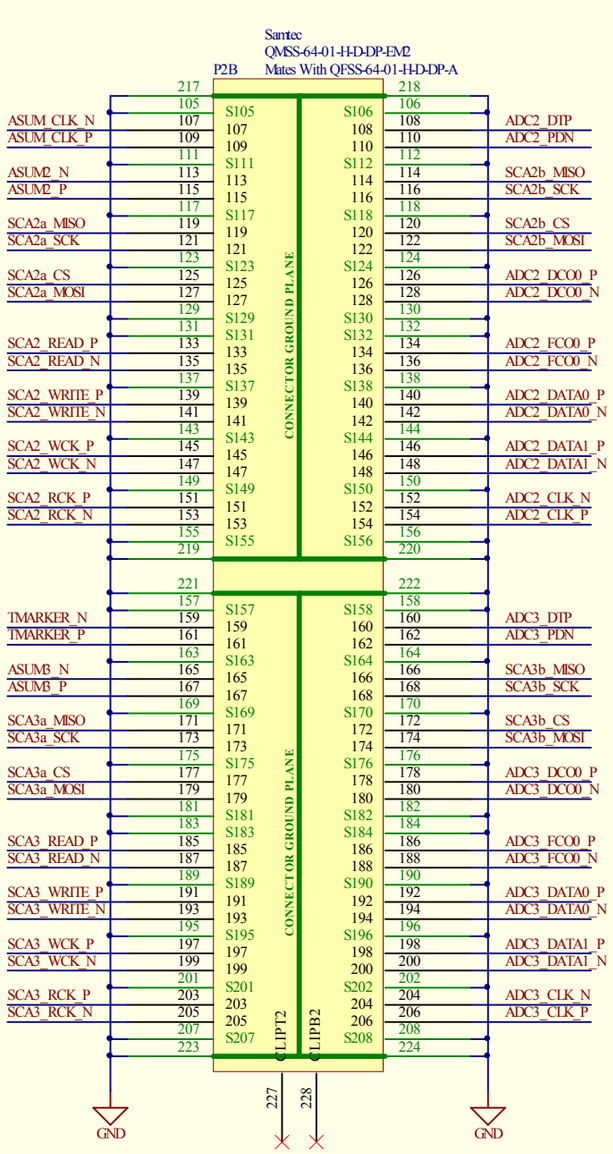
Revision B	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 3 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\ASUM_Deserializer.SchDoc			12:19:35 PM

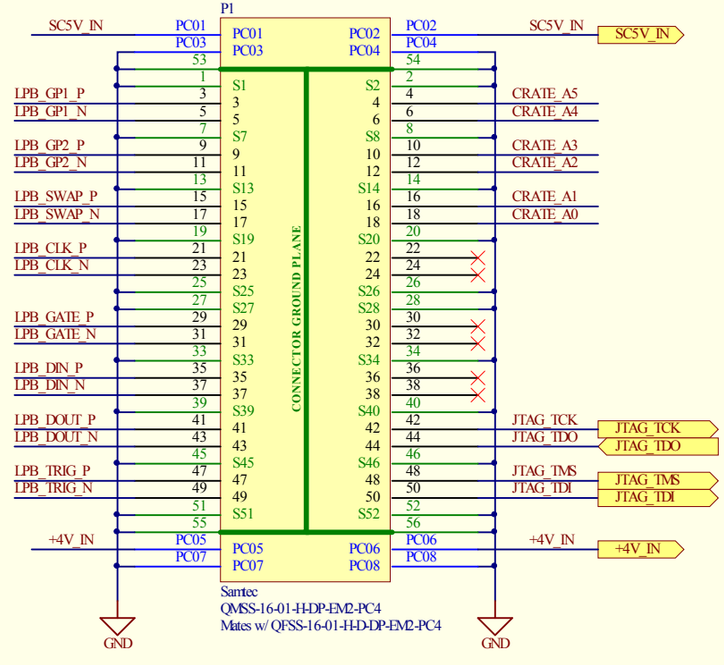


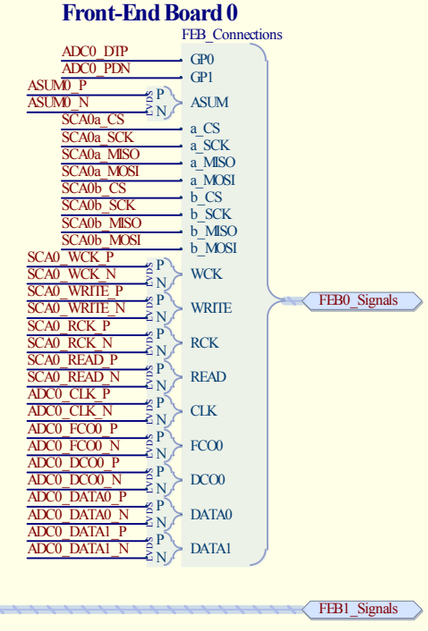
T2K_CMB - Crate Master Board (ASUM Deserializer)

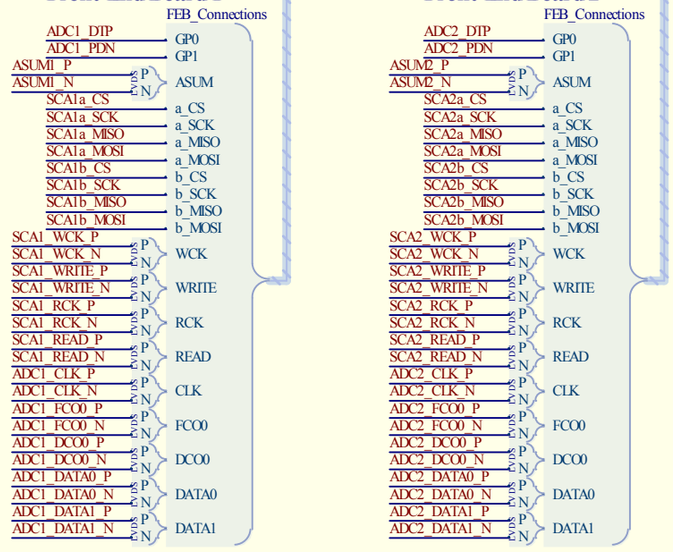
Revision B	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 3 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\ASUM_Deserializer.SchDoc			12:19:35 PM

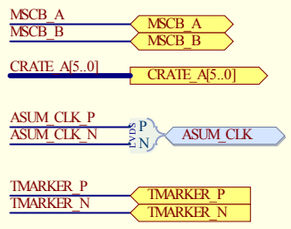


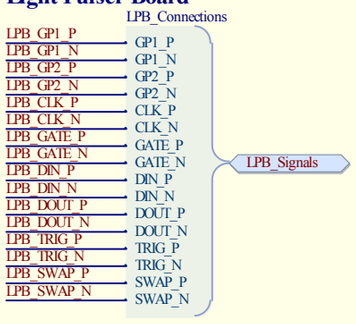






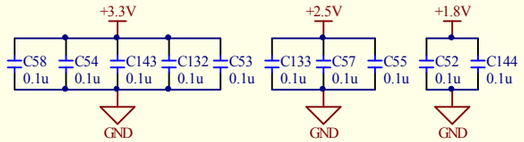




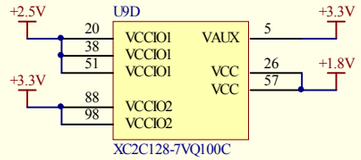


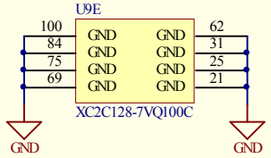
T2K_CMB - Crate Master Board (Backplane Connections)

Revision B	Drawing #: 4		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 4 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\BackplaneConnections.SchDoc			12:19:35 PM

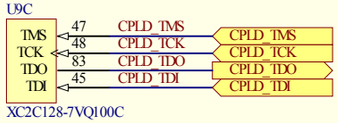


CPLD POWER/GND

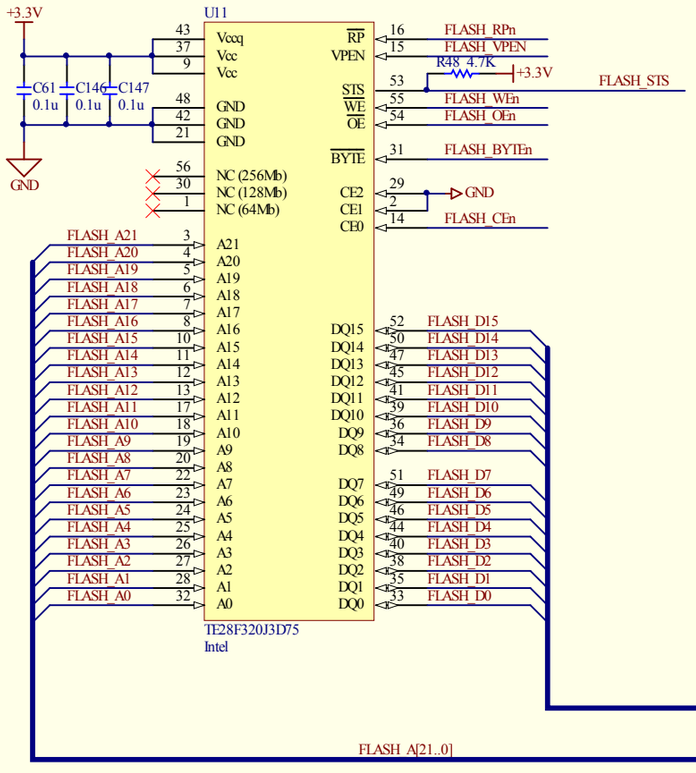




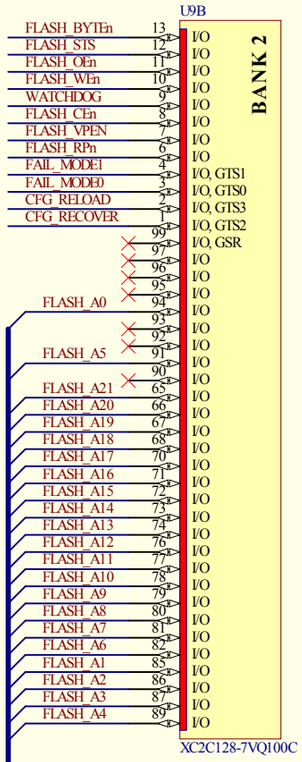
CPLD JTAG Interface



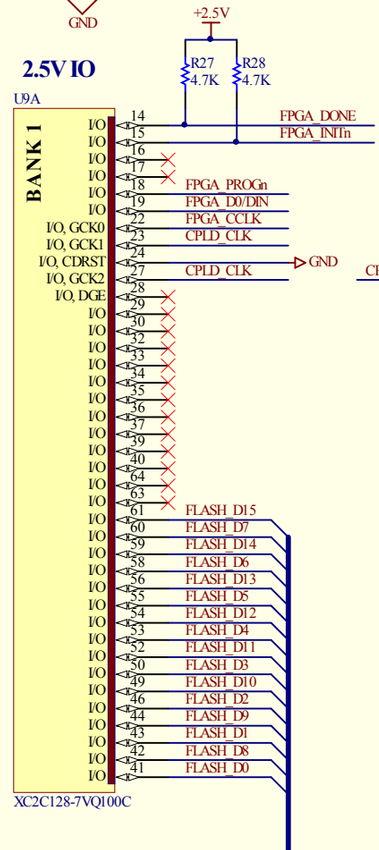
32MBit NOR FLASH

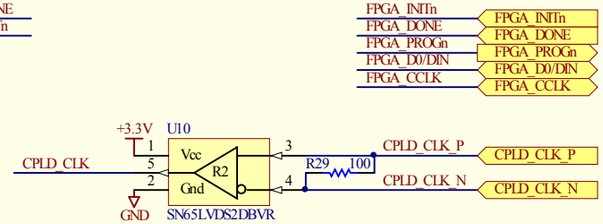


3.3V IO



2.5V IO





FLASH_D[15..0]

FLASH_A[21..0]

T2K_CMB - Crate Master Board (Configuration)			
Revision B	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\CPLDandFlashMemory.SchDoc			12:19:35 PM

Bank Voltage = +3.3V

U8A

BANK 0

IO_L01N_0/VRP_0	B24	FLASH_STS
IO_L01P_0/VRN_0	A24	FLASH_BYTEn
IO_L02N_0	D21	FLASH_D8
IO_L02P_0	C21	FLASH_OEn
IO_L03N_0	E20	FLASH_D0
IO_L03P_0/VREF_0	D20	FLASH_D1
IO_L05_0/No_Pair	F19	FLASH_D10
IO_L06N_0	E19	FLASH_D9
IO_L06P_0	E18	FLASH_D4
IO_L07N_0	D19	FLASH_D11
IO_L07P_0	C19	FLASH_D2
IO_L08N_0	B19	FLASH_WEn
IO_L08P_0	A19	WATCHDOG
IO_L09N_0	G18	FLASH_A12
IO_L09P_0/VREF_0	F18	FLASH_D12
IO_L37N_0	D18	FLASH_D3
IO_L37P_0	C18	FLASH_CEn
IO_L38N_0	G17	
IO_L38P_0	H16	FLASH_A10
IO_L39N_0	F17	FLASH_D13
IO_L39P_0	F16	FLASH_D14
IO_L43N_0	E17	FLASH_A11
IO_L43P_0	D17	FLASH_D5
IO_L44N_0	G16	
IO_L44P_0	G15	
IO_L45N_0	E16	FLASH_D6
IO_L45P_0/VREF_0	D16	FLASH_VPEN
IO_L67N_0	F15	FLASH_A21
IO_L67P_0	E15	FLASH_D15
IO_L68N_0	D15	FLASH_D7
IO_L68P_0	C15	FLASH_RPn
IO_L69N_0	H15	FLASH_A9
IO_L69P_0/VREF_0	H14	FLASH_A8
IO_L73N_0	G14	
IO_L73P_0	F14	
IO_L74N_0/GCLK7P	E14	
IO_L74P_0/GCLK6S	D14	
IO_L75N_0/GCLK5P	C14	
IO_L75P_0/GCLK4S	B14	

XC2VP7-7FF672C

Bank Voltage = +3.3V

U8B

BANK 1

IO_L75N_1/GCLK3P	B13	
IO_L75P_1/GCLK2S	C13	
IO_L74N_1/GCLK1P	D13	
IO_L74P_1/GCLK0S	E13	
IO_L73N_1	F13	
IO_L73P_1	G13	
IO_L69N_1/VREF_1	H13	FLASH_A7
IO_L69P_1	H12	FLASH_A6
IO_L68N_1	C12	FAIL_MODE1
IO_L68P_1	D12	FLASH_A18
IO_L67N_1	E12	FLASH_A19
IO_L67P_1	F12	FLASH_A20
IO_L45N_1/VREF_1	D11	FAIL_MODE0
IO_L45P_1	E11	FLASH_A17
IO_L44N_1	G12	
IO_L44P_1	G11	
IO_L43N_1	D10	FLASH_A15
IO_L43P_1	E10	FLASH_A16
IO_L39N_1	F11	FLASH_A2
IO_L39P_1	F10	FLASH_A3
IO_L38N_1	H11	FLASH_A1
IO_L38P_1	G10	
IO_L37N_1	C9	CFG_RELOAD
IO_L37P_1	D9	FLASH_A4
IO_L09N_1/VREF_1	F9	
IO_L09P_1	G9	
IO_L08N_1	A8	LOS
IO_L08P_1	B8	RateSelect
IO_L07N_1	C8	FLASH_A0
IO_L07P_1	D8	FLASH_A13
IO_L06N_1	E9	FLASH_A14
IO_L06P_1	F8	FLASH_A5
IO_L05_1/No_Pair	D7	ModDef0
IO_L03N_1/VREF_1	E7	
IO_L03P_1	C6	TX_Disable
IO_L02N_1	D6	TX_Fault
IO_L02P_1	A3	ModDef1
IO_L01N_1/VRP_1	B3	ModDef2
IO_L01P_1/VRN_1		

XC2VP7-7FF672C

Bank Voltage = +2.5V

U8C

BANK 2

IO_L01N_2/VRP_2	C4	M1_CLK
IO_L01P_2/VRN_2	D3	M1_CEn
IO_L02N_2	A2	M1_D17
IO_L02P_2	B1	M1_D16
IO_L03N_2	C2	M1_D15
IO_L03P_2	C1	M1_D14
IO_L04N_2/VREF_2	D2	M1_D13
IO_L04P_2	D1	M1_D12
IO_L05N_2	E4	M1_A16
IO_L05P_2	E3	M1_A17
IO_L06N_2	E2	M1_D11
IO_L06P_2	E1	M1_D10
IO_L43N_2	G6	M1_D18
IO_L43P_2	G5	M1_D19
IO_L44N_2	G4	M1_D20
IO_L44P_2	G3	M1_D9
IO_L45N_2	F1	M1_ZZ
IO_L45P_2	G1	M1_D8
IO_L46N_2/VREF_2	H6	M1_A3
IO_L46P_2	H5	M1_A2
IO_L47N_2	H4	M1_A15
IO_L47P_2	H3	M1_D22
IO_L48N_2	H2	M1_D7
IO_L48P_2	H1	M1_D6
IO_L49N_2	J7	M1_A13
IO_L49P_2	J6	M1_A14
IO_L50N_2	J5	M1_D21
IO_L50P_2	J4	M1_D23
IO_L51N_2	J3	M1_A4
IO_L51P_2	J2	M1_D5
IO_L52N_2/VREF_2	K6	M1_A18
IO_L52P_2	K5	M1_LDn
IO_L53N_2	K4	M1_A5
IO_L53P_2	K3	M1_A1
IO_L54N_2	J1	M1_D4
IO_L54P_2	K1	M1_D3
IO_L55N_2	K7	M1_D24
IO_L55P_2	L8	M1_D25
IO_L56N_2	L7	M1_CENn
IO_L56P_2	M7	M1_WEn
IO_L57N_2	L6	M1_A19
IO_L57P_2	L5	M1_A0
IO_L58N_2/VREF_2	L4	M1_OEn
IO_L58P_2	L3	M1_D26
IO_L59N_2	L2	M1_D2
IO_L59P_2	L1	M1_D1
IO_L60N_2	M8	M1_D29
IO_L60P_2	N8	M1_D30
IO_L85N_2	M6	M1_D28
IO_L85P_2	M5	M1_D27
IO_L86N_2	M4	M1_A7
IO_L86P_2	M3	M1_A6
IO_L87N_2	M2	M1_D0
IO_L87P_2	M1	M1_A12
IO_L88N_2/VREF_2	N7	M1_BW1n
IO_L88P_2	N6	M1_BW0n
IO_L89N_2	N5	M1_A10
IO_L89P_2	N4	M1_A9
IO_L90N_2	N3	M1_A8
IO_L90P_2	N2	M1_A11

XC2VP7-7FF672C

Bank Voltage = +2.5V

U8D

BANK 3

IO_L90N_3	P2	M2_A18
IO_L90P_3	P3	M2_CENn
IO_L89N_3	P4	M2_WEn
IO_L89P_3	P5	M2_CLK
IO_L88N_3	P6	M1_BW3n
IO_L88P_3	P7	M1_BW2n
IO_L87N_3/VREF_3	R1	M2_A15
IO_L87P_3	R2	M2_A14
IO_L86N_3	R3	M2_OEn
IO_L86P_3	R4	M2_LDn
IO_L85N_3	R5	M1_D34
IO_L85P_3	R6	M1_D33
IO_L60N_3	P8	M1_D31
IO_L60P_3	R8	M1_D32
IO_L59N_3	T1	M2_A13
IO_L59P_3	T2	M2_D17
IO_L58N_3	T3	M1_D35
IO_L58P_3	T4	M2_A4
IO_L57N_3/VREF_3	T5	M2_BW1n
IO_L57P_3	T6	M2_BW0n
IO_L56N_3	R7	M2_A2
IO_L56P_3	T7	M2_A3
IO_L55N_3	T8	M2_D18
IO_L55P_3	U7	M2_D19
IO_L54N_3	U1	M2_D16
IO_L54P_3	V1	M2_D15
IO_L53N_3	U3	M2_BW2n
IO_L53P_3	U4	M2_BW3n
IO_L52N_3	U5	M2_A5
IO_L52P_3	U6	M2_A1
IO_L51N_3/VREF_3	V2	M2_D14
IO_L51P_3	V3	M2_CEn
IO_L50N_3	V4	M2_D20
IO_L50P_3	V5	M2_D22
IO_L49N_3	V6	M2_A19
IO_L49P_3	V7	M2_A6
IO_L48N_3	W1	M2_D13
IO_L48P_3	W2	M2_D12
IO_L47N_3	W3	M2_D21
IO_L47P_3	W4	M2_A0
IO_L46N_3	W5	M2_A17
IO_L46P_3	W6	M2_A16
IO_L45N_3/VREF_3	Y1	M2_D11
IO_L45P_3	AA1	M2_D10
IO_L44N_3	Y3	M2_D9
IO_L44P_3	Y4	M2_D23
IO_L43N_3	Y5	M2_D24
IO_L43P_3	Y6	M2_D25
IO_L06N_3	AB3	M2_ZZ
IO_L06P_3	AB4	M2_D26
IO_L05N_3	AC1	M2_D8
IO_L05P_3	AC2	M2_D7
IO_L04N_3	AD1	M2_D6
IO_L04P_3	AD2	M2_D5
IO_L03N_3/VREF_3	AE1	M2_D4
IO_L03P_3	AF2	M2_D3
IO_L02N_3	AC3	M2_D28
IO_L02P_3	AD4	M2_D0
IO_L01N_3/VRP_3	AE3	M2_D2
IO_L01P_3/VRN_3	AF3	M2_D1

XC2VP7-7FF672C

CFG_RELOAD
WATCHDOG
FAIL_MODE[1..0]

TX_Fault
TX_Disable
ModDef2
ModDef1
ModDef0
RateSelect
LOS

FLASH_A[21..0]
FLASH_D[15..0]
FLASH_STS
FLASH_CEn
FLASH_OEn
FLASH_WEn
FLASH_VPEN
FLASH_RPn
FLASH_BYTEn

M1_A[19..0]
M1_D[35..0]

M1_LDn
M1_CLK
M1_CENn
M1_CEn
M1_OEn
M1_WEn
M1_ZZ
M1_BW0n
M1_BW1n
M1_BW2n
M1_BW3n

M2_A[19..0]
M2_D[35..0]

M2_LDn
M2_CLK
M2_CENn
M2_CEn
M2_OEn
M2_WEn
M2_ZZ
M2_BW0n
M2_BW1n
M2_BW2n
M2_BW3n

T2K_CMB - Crate Master Board (FPGA - IO Bank 0-3)

Revision B	Drawing #: 6		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 6 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\FPGA_IOBank0-3.SchDoc			12:19:35 PM

Bank Voltage = +2.5V

U8E

BANK 4

IO_L01N_4/DOUT	AC6	M2_D30
IO_L01P_4/INIT_B	AD6	FPGA_INITn
IO_L02N_4/D0	AB7	FPGA_D0/DIN
IO_L02P_4/D1	AC7	M2_D31
IO_L03N_4/D2	AA7	M2_D27
IO_L03P_4/D3	AA8	M2_A8
IO_L05_4/No_Pair	Y8	M2_A7
IO_L06N_4/VRP_4	AB8	M2_D29
IO_L06P_4/VRN_4	AB9	M2_D33
IO_L07N_4	AC8	M2_D32
IO_L07P_4/VREF_4	AD8	M2_D34
IO_L08N_4	AE8	M2_A12
IO_L08P_4	AF8	M2_A11
IO_L09N_4	Y9	M2_A9
IO_L09P_4/VREF_4	AA9	
IO_L37N_4	AC9	M2_D35
IO_L37P_4	AD9	M2_A10
IO_L38N_4	Y10	LPB_TRIG_N
IO_L38P_4	W11	LPB_TRIG_P
IO_L39N_4	AA10	LPB_DIN_N
IO_L39P_4	AA11	LPB_DIN_P
IO_L43N_4	AB10	LPB_DOUT_N
IO_L43P_4	AC10	LPB_DOUT_P
IO_L44N_4	Y11	
IO_L44P_4	Y12	
IO_L45N_4	AB11	LPB_GATE_N
IO_L45P_4/VREF_4	AC11	LPB_GATE_P
IO_L67N_4	AA12	LPB_CLK_N
IO_L67P_4	AB12	LPB_CLK_P
IO_L68N_4	AC12	LPB_SWAP_N
IO_L68P_4	AD12	LPB_SWAP_P
IO_L69N_4	W12	LPB_GP2_N
IO_L69P_4/VREF_4	W13	LPB_GP2_P
IO_L73N_4	Y13	LPB_GP1_N
IO_L73P_4	AA13	LPB_GP1_P
IO_L74N_4/GCLK3S	AB13	
IO_L74P_4/GCLK2P	AC13	
IO_L75N_4/GCLK1S	AD13	FPGA_CLK_N
IO_L75P_4/GCLK0P	AE13	FPGA_CLK_P

XC2VP7-7FF672C

Bank Voltage = +3.3V

U8F

BANK 5

IO_L75N_5/GCLK7S	AE14	
IO_L75P_5/GCLK6P	AD14	SCA3b_CS
IO_L74N_5/GCLK5S	AC14	SCA3a_MISO
IO_L74P_5/GCLK4P	AB14	SCA3a_SCK
IO_L73N_5	AA14	SCA3b_MOSI
IO_L73P_5	Y14	SCA2a_CS
IO_L69N_5/VREF_5	W14	SCA3a_MOSI
IO_L69P_5	W15	SCA2a_MOSI
IO_L68N_5	AD15	SCA2a_MISO
IO_L68P_5	AC15	SCA2b_CS
IO_L67N_5	AB15	SCA3b_SCK
IO_L67P_5	AA15	SCA2a_SCK
IO_L45N_5/VREF_5	AC16	SCA2b_SCK
IO_L45P_5	AB16	ADC3_PDN
IO_L44N_5	Y15	SCA3a_CS
IO_L44P_5	Y16	CRATE_A1
IO_L43N_5	AC17	ADC2_PDN
IO_L43P_5	AB17	ADC3_DTP0
IO_L39N_5	AA16	SCA3b_MISO
IO_L39P_5	AA17	CRATE_A3
IO_L38N_5	W16	SCA2b_MOSI
IO_L38P_5	Y17	CRATE_A2
IO_L37N_5	AD18	SCA1a_MOSI
IO_L37P_5	AC18	ADC2_DTP0
IO_L09N_5/VREF_5	AA18	CRATE_A4
IO_L09P_5	Y18	CRATE_A0
IO_L08N_5	AF19	SCA2b_MISO
IO_L08P_5	AE19	SCA1a_SCK
IO_L07N_5/VREF_5	AD19	SCA0a_MOSI
IO_L07P_5	AC19	SCA0a_CS
IO_L06N_5/VRP_5	AB18	SCA1a_CS
IO_L06P_5/VRN_5	AB19	SCA1b_MOSI
IO_L05_5/No_Pair	Y19	CRATE_A5
IO_L03N_5/D4	AA19	SCA1b_CS
IO_L03P_5/D5	AA20	SCA1b_MISO
IO_L02N_5/D6	AC20	SCA0b_MOSI
IO_L02P_5/D7	AB20	SCA1a_MISO
IO_L01N_5/RDWR_B	AD21	SCA0a_SCK
IO_L01P_5/CS_B	AC21	SCA0a_MISO

XC2VP7-7FF672C

Bank Voltage = +3.3V

U8G

BANK 6

IO_L01P_6/VRN_6	AF24	SCA0b_CS
IO_L01N_6/VRP_6	AE24	SCA1b_SCK
IO_L02P_6	AD23	SCA0b_MISO
IO_L02N_6	AC24	ADC0_PDN
IO_L03P_6	AE26	ADC0_DTP0
IO_L03N_6/VREF_6	AF25	ADC1_DTP0
IO_L04P_6	AD25	ADC1_PDN
IO_L04N_6	AD26	SUM3_RCLK
IO_L05P_6	AC25	SUM3_PWRDNn
IO_L05N_6	AC26	SUM2_RCLK
IO_L06P_6	AB23	SCA0b_SCK
IO_L06N_6	AB24	SUM2_PWRDNn
IO_L43P_6	Y21	SUM3_D2
IO_L43N_6	Y22	SUM2_D3
IO_L44P_6	Y23	SUM3_D4
IO_L44N_6	Y24	SUM3_D5
IO_L45P_6	AA26	SUM3_LOCKn
IO_L45N_6/VREF_6	Y26	SUM2_LOCKn
IO_L46P_6	W21	SUM2_D2
IO_L46N_6	W22	SUM2_D4
IO_L47P_6	W23	SUM3_D6
IO_L47N_6	W24	SUM2_D6
IO_L48P_6	W25	SUM3_D0
IO_L48N_6	W26	SUM2_D0
IO_L49P_6	V20	SUM3_D3
IO_L49N_6	V21	SUM3_D7
IO_L50P_6	V22	SUM2_D5
IO_L50N_6	V23	SUM1_PWRDNn
IO_L51P_6	V24	SUM0_PWRDNn
IO_L51N_6/VREF_6	V25	SUM3_D1
IO_L52P_6	U21	SC_DEBUG2
IO_L52N_6	U22	SUM2_D7
IO_L53P_6	U23	SUM0_RCLK
IO_L53N_6	U24	SUM0_D1
IO_L54P_6	V26	SUM2_D1
IO_L54N_6	U26	
IO_L55P_6	U20	SC_DEBUG1
IO_L55N_6	T19	SC_DEBUG0
IO_L56P_6	T20	ADC3_DTP1
IO_L56N_6	R20	ADC1_DTP1
IO_L57P_6	T21	SUM0_D2
IO_L57N_6/VREF_6	T22	SUM1_RCLK
IO_L58P_6	T23	SUM0_D3
IO_L58N_6	T24	SUM1_D1
IO_L59P_6	T25	SUM1_D0
IO_L59N_6	T26	SUM1_LOCKn
IO_L60P_6	R19	ADC2_DTP1
IO_L60N_6	P19	ADC0_DTP1
IO_L85P_6	R21	SUM1_D2
IO_L85N_6	R22	SUM0_D5
IO_L86P_6	R23	SUM1_D3
IO_L86N_6	R24	SUM0_D4
IO_L87P_6	R25	SUM0_LOCKn
IO_L87N_6/VREF_6	R26	SUM0_D0
IO_L88P_6	P20	SUM0_D7
IO_L88N_6	P21	SUM0_D6
IO_L89P_6	P22	SUM1_D7
IO_L89N_6	P23	SUM1_D6
IO_L90P_6	P24	SUM1_D4
IO_L90N_6	P25	SUM1_D5

XC2VP7-7FF672C

Bank Voltage = +2.5V

U8H

BANK 7

IO_L90P_7	N25	ADC2_CLK_P
IO_L90N_7	N24	ADC2_CLK_N
IO_L89P_7	N23	ADC3_DATA1_P
IO_L89N_7	N22	ADC3_DATA1_N
IO_L88P_7	N21	ADC3_DATA0_P
IO_L88N_7/VREF_7	N20	ADC3_DATA0_N
IO_L87P_7	M26	ADC3_FCO0_P
IO_L87N_7	M25	ADC3_FCO0_N
IO_L86P_7	M24	ADC2_DATA1_P
IO_L86N_7	M23	ADC2_DATA1_N
IO_L85P_7	M22	ADC3_DCO0_P
IO_L85N_7	M21	ADC3_DCO0_N
IO_L60P_7	N19	ADC3_CLK_P
IO_L60N_7	M19	ADC3_CLK_N
IO_L59P_7	L26	ADC2_FCO0_P
IO_L59N_7	L25	ADC2_FCO0_N
IO_L58P_7	L24	ADC2_DATA0_P
IO_L58N_7/VREF_7	L23	ADC2_DATA0_N
IO_L57P_7	L22	ADC2_DCO0_P
IO_L57N_7	L21	ADC2_DCO0_N
IO_L56P_7	M20	
IO_L56N_7	L20	
IO_L55P_7	L19	
IO_L55N_7	K20	
IO_L54P_7	K26	ADC1_CLK_P
IO_L54N_7	J26	ADC1_CLK_N
IO_L53P_7	K24	ADC1_DATA1_P
IO_L53N_7	K23	ADC1_DATA1_N
IO_L52P_7	K22	
IO_L52N_7/VREF_7	K21	
IO_L51P_7	J25	ADC1_DCO0_P
IO_L51N_7	J24	ADC1_DCO0_N
IO_L50P_7	J23	ADC1_DATA0_P
IO_L50N_7	J22	ADC1_DATA0_N
IO_L49P_7	J21	
IO_L49N_7	J20	
IO_L48P_7	H26	ADC0_CLK_P
IO_L48N_7	H25	ADC0_CLK_N
IO_L47P_7	H24	ADC0_DATA1_P
IO_L47N_7	H23	ADC0_DATA1_N
IO_L46P_7	H22	ADC1_FCO0_P
IO_L46N_7/VREF_7	H21	ADC1_FCO0_N
IO_L45P_7	G26	ADC0_DATA0_P
IO_L45N_7	F26	ADC0_DATA0_N
IO_L44P_7	G24	SCA_READ_P
IO_L44N_7	G23	SCA_READ_N
IO_L43P_7	G22	SCA_RCK_P
IO_L43N_7	G21	SCA_RCK_N
IO_L06P_7	E26	ASUM_CLK_P
IO_L06N_7	E25	ASUM_CLK_N
IO_L05P_7	E24	ADC0_FCO0_P
IO_L05N_7	E23	ADC0_FCO0_N
IO_L04P_7	D26	SCA_WCK_P
IO_L04N_7/VREF_7	D25	SCA_WCK_N
IO_L03P_7	C26	SCA_WRITE_P
IO_L03N_7	C25	SCA_WRITE_N
IO_L02P_7	B26	TRIGOUT_P
IO_L02N_7	A25	TRIGOUT_N
IO_L01P_7/VRN_7	D24	ADC0_DCO0_P
IO_L01N_7/VRP_7	C23	ADC0_DCO0_N

XC2VP7-7FF672C

Front-End Board 1

FEB_Connections

ADC1_DTP	GP0		
ADC1_PDN	GP1		
ASUM1_P	P	ASUM	
ASUM1_N	N		
SCA1a_CS		a_CS	
SCA1a_SCK		a_SCK	
SCA1a_MISO		a_MISO	
SCA1a_MOSI		a_MOSI	
SCA1b_CS		b_CS	
SCA1b_SCK		b_SCK	
SCA1b_MISO		b_MISO	
SCA1b_MOSI		b_MOSI	
SCA1_WCK_P	P	WCK	
SCA1_WCK_N	N		
SCA1_WRITE_P	P	WRITE	
SCA1_WRITE_N	N		
SCA1_RCK_P	P	RCK	
SCA1_RCK_N	N		
SCA1_READ_P	P	READ	
SCA1_READ_N	N		
ADC1_CLK_P	P	CLK	
ADC1_CLK_N	N		
ADC1_FCO0_P	P	FCO0	
ADC1_FCO0_N	N		
ADC1_DCO0_P	P	DCO0	
ADC1_DCO0_N	N		
ADC1_DATA0_P	P	DATA0	
ADC1_DATA0_N	N		
ADC1_DATA1_P	P	DATA1	
ADC1_DATA1_N	N		

Front-End Board 0

FEB_Connections

ADC0_DTP	GP0		
ADC0_PDN	GP1		
ASUM0_P	P	ASUM	
ASUM0_N	N		
SCA0a_CS		a_CS	
SCA0a_SCK		a_SCK	
SCA0a_MISO		a_MISO	
SCA0a_MOSI		a_MOSI	
SCA0b_CS		b_CS	
SCA0b_SCK		b_SCK	
SCA0b_MISO		b_MISO	
SCA0b_MOSI		b_MOSI	
SCA0_WCK_P	P	WCK	
SCA0_WCK_N	N		
SCA0_WRITE_P	P	WRITE	
SCA0_WRITE_N	N		
SCA0_RCK_P	P	RCK	
SCA0_RCK_N	N		
SCA0_READ_P	P	READ	
SCA0_READ_N	N		
ADC0_CLK_P	P	CLK	
ADC0_CLK_N	N		
ADC0_FCO0_P	P	FCO0	
ADC0_FCO0_N	N		
ADC0_DCO0_P	P	DCO0	
ADC0_DCO0_N	N		
ADC0_DATA0_P	P	DATA0	
ADC0_DATA0_N	N		
ADC0_DATA1_P	P	DATA1	
ADC0_DATA1_N	N		

FEB0_Signals

FEB1_Signals

FEB2_Signals

Front-End Board 2

FEB_Connections

ADC2_DTP	GP0		
ADC2_PDN	GP1		
ASUM2_P	P	ASUM	
ASUM2_N	N		
SCA2a_CS		a_CS	
SCA2a_SCK		a_SCK	
SCA2a_MISO		a_MISO	
SCA2a_MOSI		a_MOSI	
SCA2b_CS		b_CS	
SCA2b_SCK		b_SCK	
SCA2b_MISO		b_MISO	
SCA2b_MOSI		b_MOSI	
SCA2_WCK_P	P	WCK	
SCA2_WCK_N	N		
SCA2_WRITE_P	P	WRITE	
SCA2_WRITE_N	N		
SCA2_RCK_P	P	RCK	
SCA2_RCK_N	N		
SCA2_READ_P	P	READ	
SCA2_READ_N	N		
ADC2_CLK_P	P	CLK	
ADC2_CLK_N	N		
ADC2_FCO0_P	P	FCO0	
ADC2_FCO0_N	N		
ADC2_DCO0_P	P	DCO0	
ADC2_DCO0_N	N		
ADC2_DATA0_P	P	DATA0	
ADC2_DATA0_N	N		
ADC2_DATA1_P	P	DATA1	
ADC2_DATA1_N	N		

Front-End Board 3

FEB_Connections

ADC3_DTP	GP0		
ADC3_PDN	GP1		
ASUM3_P	P	ASUM	
ASUM3_N	N		
SCA3a_CS		a_CS	
SCA3a_SCK		a_SCK	
SCA3a_MISO		a_MISO	
SCA3a_MOSI		a_MOSI	
SCA3b_CS		b_CS	
SCA3b_SCK		b_SCK	
SCA3b_MISO		b_MISO	
SCA3b_MOSI		b_MOSI	
SCA3_WCK_P	P	WCK	
SCA3_WCK_N	N		
SCA3_WRITE_P	P	WRITE	
SCA3_WRITE_N	N		
SCA3_RCK_P	P	RCK	
SCA3_RCK_N	N		
SCA3_READ_P	P	READ	
SCA3_READ_N	N		
ADC3_CLK_P	P	CLK	
ADC3_CLK_N	N		
ADC3_FCO0_P	P	FCO0	
ADC3_FCO0_N	N		
ADC3_DCO0_P	P	DCO0	
ADC3_DCO0_N	N		
ADC3_DATA0_P	P	DATA0	
ADC3_DATA0_N	N		
ADC3_DATA1_P	P	DATA1	
ADC3_DATA1_N	N		

FEB3_Signals

CRATE_A[5..0] → CRATE_A[5..0]

Light Pulser Board

LPB_Connections

LPB_GP1_P	GP1_P	
LPB_GP1_N	GP1_N	
LPB_GP2_P	GP2_P	
LPB_GP2_N	GP2_N	
LPB_CLK_P	CLK_P	
LPB_CLK_N	CLK_N	
LPB_GATE_P	GATE_P	
LPB_GATE_N	GATE_N	
LPB_DIN_P	DIN_P	
LPB_DIN_N	DIN_N	
LPB_DOUT_P	DOUT_P	
LPB_DOUT_N	DOUT_N	
LPB_TRIG_P	TRIG_P	
LPB_TRIG_N	TRIG_N	
LPB_SWAP_P	SWAP_P	
LPB_SWAP_N	SWAP_N	

LPB_Signals

RCK
LVDSFanout1to4.SchDoc
SCA_RCK_P → SCA0_RCK_P, SCA0_RCK_N, SCA1_RCK_P, SCA1_RCK_N, SCA2_RCK_P, SCA2_RCK_N, SCA3_RCK_P, SCA3_RCK_N
SCA_RCK_N

READ
LVDSFanout1to4.SchDoc
SCA_READ_P → SCA0_READ_P, SCA0_READ_N, SCA1_READ_P, SCA1_READ_N, SCA2_READ_P, SCA2_READ_N, SCA3_READ_P, SCA3_READ_N
SCA_READ_N

WCK
LVDSFanout1to4.SchDoc
SCA_WCK_P → SCA0_WCK_P, SCA0_WCK_N, SCA1_WCK_P, SCA1_WCK_N, SCA2_WCK_P, SCA2_WCK_N, SCA3_WCK_P, SCA3_WCK_N
SCA_WCK_N

WRITE
LVDSFanout1to4.SchDoc
SCA_WRITE_P → SCA0_WRITE_P, SCA0_WRITE_N, SCA1_WRITE_P, SCA1_WRITE_N, SCA2_WRITE_P, SCA2_WRITE_N, SCA3_WRITE_P, SCA3_WRITE_N
SCA_WRITE_N

FPGA_CLK_P → FPGA_CLK_P
FPGA_CLK_N → FPGA_CLK_N

TRIGOUT_P → TRIGOUT_P
TRIGOUT_N → TRIGOUT_N

FPGA_INITn → FPGA_INITn
FPGA_D0/DIN → FPGA_D0/DIN

ASUM_CLK_P, ASUM_CLK_N → ASUM_CLK

SUM0_D[7..0] → SUM0_D[7..0]
SUM0_RCLK → SUM0_RCLK
SUM0_LOCKn → SUM0_LOCKn
SUM0_PWRDNn → SUM0_PWRDNn

SUM1_D[7..0] → SUM1_D[7..0]
SUM1_RCLK → SUM1_RCLK
SUM1_LOCKn → SUM1_LOCKn
SUM1_PWRDNn → SUM1_PWRDNn

SUM2_D[7..0] → SUM2_D[7..0]
SUM2_RCLK → SUM2_RCLK
SUM2_LOCKn → SUM2_LOCKn
SUM2_PWRDNn → SUM2_PWRDNn

SUM3_D[7..0] → SUM3_D[7..0]
SUM3_RCLK → SUM3_RCLK
SUM3_LOCKn → SUM3_LOCKn
SUM3_PWRDNn → SUM3_PWRDNn

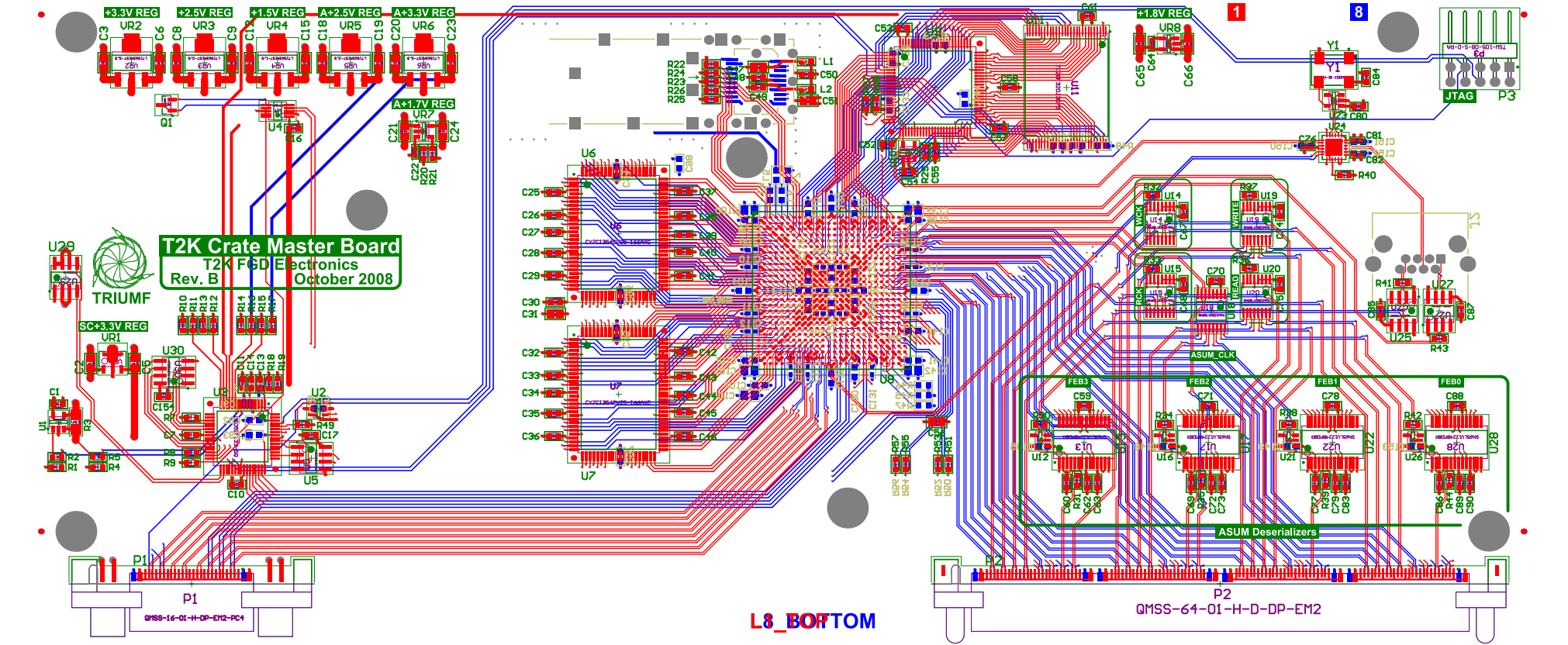
M2_A[19..0] → M2_A[19..0]
M2_D[35..0] → M2_D[35..0]

ADC0_DTP1	R50 4.7K	ADC0_DTP
ADC0_DTP0	R51 10K	
ADC1_DTP1	R52 4.7K	ADC1_DTP
ADC1_DTP0	R53 10K	
ADC2_DTP1	R54 4.7K	ADC2_DTP
ADC2_DTP0	R55 10K	
ADC3_DTP1	R56 4.7K	ADC3_DTP
ADC3_DTP0	R57 10K	

SC_DEBUG[2..0] → SC_DEBUG[2..0]

T2K_CMB - Crate Master Board (FPGA - IO Bank 4-7)

Revision B	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 7 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 18/12/2008	
File: M:\edevel\Altium\Projects\T2K_CMB_RevB\FPGA_IOBank4-7.SchDoc			12:19:36 PM


+3.3V REG
+2.5V REG
+1.5V REG
A+2.5V REG
A+3.3V REG
A+1.7V REG
+1.8V REG
SC+3.3V REG
T2K Crate Master Board
T2K FGD Electronics
Rev. B
October 2008
TRIUMF
JTAG
ASUM_CLK
ASUM Deserializers
FEB3
FEB2
FEB1
FEB0
P1
QMSS-16-01-H-DP-EM2-PC1
P2
QMSS-64-01-H-D-DP-EM2
L8_BOTTOM